



M S Ramaiah University of Applied Sciences

**Program Structure and Course Details
of
M.Tech (VLSI and Nanotechnology) Degree
Programme**

Programme Code: 120

Batch: 2019 Onwards

**Department of Electronics and Communication Engineering
Faculty of Engineering and Technology
M S Ramaiah University of Applied Sciences**



Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019

Page 1 of 94

Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 054

Academic Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 054

University's Vision, Mission and Objectives

The M. S. Ramaiah University of Applied Sciences (MSRUAS) will focus on student-centric professional education and motivates its staff and students to contribute significantly to the growth of technology, science, economy and society through their imaginative, creative and innovative pursuits. Hence, the University has articulated the following vision and objectives.

Vision

MSRUAS aspires to be the premier university of choice in Asia for student centric professional education and services with a strong focus on applied research whilst maintaining the highest academic and ethical standards in a creative and innovative environment


Mission

Our purpose is the creation and dissemination of knowledge. We are committed to creativity, innovation and excellence in our teaching and research. We value integrity, quality and teamwork in all our endeavors. We inspire critical thinking, personal development and a passion for lifelong learning. We serve the technical, scientific and economic needs of our Society.


Objectives

1. To disseminate knowledge and skills through instructions, teaching, training, seminars, workshops and symposia in Engineering and Technology, Art and Design, Management and Commerce, Health and Allied Sciences, Physical and Life Sciences, Arts, Humanities and Social Sciences to equip students and scholars to meet the needs of industries, business and society
2. To generate knowledge through research in Engineering and Technology, Art and Design, Management and Commerce, Health and Allied Sciences, Physical and Life Sciences, Arts, Humanities and Social Sciences to meet the challenges that arise in industry, business and society
3. To promote health, human well-being and provide holistic healthcare
4. To provide technical and scientific solutions to real life problems posed by industry, business and society in Engineering and Technology, Art and Design, Management and Commerce, Health and Allied Sciences, Physical and Life Sciences, Arts, Humanities and Social Sciences
5. To instill the spirit of entrepreneurship in our youth to help create more career opportunities in the society by incubating and nurturing technology product ideas and supporting technology backed business
6. To identify and nurture leadership skills in students and help in the development of our future leaders to enrich the society we live in
7. To develop partnership with universities, industries, businesses, research establishments, NGOs, international organizations, governmental organizations in India and abroad to enrich the experiences of faculties and students through research and developmental programmes

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019


Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 054

Page 2 of 94


Academic Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 054

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

Programme Specifications: B. Tech. (Electronics and Communication Engineering)

Faculty	Engineering and Technology
Department	Electronics and Communication Engineering
Programme Code	120
Programme Name	M.Tech. (VLSI and Nanotechnology)
Dean of the Faculty	Prof. H. M. Rajashekara Swamy
Head of the Department	Dr. S. Malathi

1. **Title of the Award:** M.Tech. (VLSI and Nanotechnology)
2. **Mode of Study:** Full-Time
3. **Awarding Institution /Body:** M. S. Ramaiah University of Applied Sciences, Bengaluru
4. **Joint Award:** Not Applicable
5. **Teaching Institution:** Faculty of Engineering and Technology, M. S. Ramaiah University of Applied Sciences, Bengaluru
6. **Date of Programme Specifications:** October 2020
7. **Date of Programme Approval by the Academic Council of MSRUAS:** 23-Oct-2020
8. **Next Review Date:** May 2022
9. **Programme Approving Regulating Body and Date of Approval:** All India Council for Technical Education, New Delhi, 30-Jun-2020
10. **Programme Accredited Body and Date of Accreditation:** Not Applicable
11. **Grade Awarded by the Accreditation Body:** Not Applicable
12. **Programme Accreditation Validity:** Not Applicable
13. **Programme Benchmark:** Not Applicable
14. **Rationale for the Programme**

The theoretical developments that occurred in previous centuries in understanding electromagnetic fields and material properties have ushered the growth in the domain of Electronics and Communication during the first half of twentieth century. The second half has seen innovation and novelty in chip technology and telecommunication. Communication technology has resulted in a major societal revolution in developing countries such as India. There is a need for highly trained manpower in the domain of Electronics and Communication engineering. Good outcome-based undergraduate engineering education is critical in developing human resources.

The National Association of Software and Services Companies (NASSCOM) study, conducted in 2010 and titled "Global Engineering Research and Development: Accelerating Innovation with Indian Engineering", underlined the significance for India as the country has posted a revenue growth of about 40% during 2007-2010 and is expected to grow in coming years.

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019


Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 054


Academic Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 054

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

The Electronics and Communication Engineering programme at Faculty of Engineering and Technology at MSRUAS has been developed by the members of the faculty based on their teaching experience and long-standing interactions with various universities and industries in India and abroad.

The outcome-based curriculum helps students to develop critical thinking abilities and imbibe relevant practical skills for a smooth transition from academics to real-life work environments. Opportunities are provided for the students to do their internship in India or abroad depending on their preferences.

The Global Innovation 1000, reported in 2012, by management consulting firm Booz & Company has indicated that R & D investment in Computing, Electronics, Tele-communication is about 30% by top innovative companies making this sector a leader. The importance of technological advancements in electronics could also be seen in other categories such as Automobile, Process industries, etc. Expertise needs to be built for the design, analysis, simulation, testing and evaluation of analog, digital, control, instrumentation, and communication systems. In the light of above, knowledge of computer architectures and communication protocols is required. Outcome based undergraduate programme along with modern pedagogy is the need of the hour.

The programme provides strong foundation in basic concepts, followed by comprehensive understanding of electrical, electronics, and communication courses. Emphasis is laid on simulation, and larger perspective of systems and sub-systems of electronic products. Students are trained to develop life-long skills to understand, analyse, and develop solutions for challenging technological problems.

There is a shortage of quality electronics and communication graduates despite many institutions offering undergraduate programmes. The FET at MSRUAS would like to offer Electronics and Communication Engineering programme to produce imaginative, creative, and innovative engineers to solve the problems of the society.

15. Programme Mission

The purpose of the programme is to create innovative problem solvers in multi-disciplinary settings, entrepreneurs and leaders that apply their knowledge, understanding, cognitive abilities, practical skills and transferable skills gained through systematic, flexible and rigorous learning in the chosen academic domain.

16. Graduate Attributes (GAs)

GA-1. Scholarship of Knowledge: Ability to apply knowledge of mathematics, science, and Engineering fundamentals to solve complex problems in engineering

GA-2. Critical thinking: Ability to analyse engineering problems, interpret data and arrive at meaningful conclusions involving mathematical inferences

GA-3. Problem Solving: Ability to design an engineering system, component, or process to meet desired needs considering public health and safety, and the cultural, societal, and environmental considerations



Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

- GA-4. Research Skill:** Ability to understand and solve complex engineering problems by conducting experimental investigations
- GA-5. Usage of Modern Tools:** Ability to apply appropriate tools and techniques and understand utilization of resources appropriately to complex engineering activities
- GA-6. Collaborative and Multi-disciplinary work:** Ability to understand the effect of engineering solutions on legal, cultural, social, and public health and safety aspects
- GA-7. Social Responsibility:** Ability to develop sustainable solutions and understand their effect on society and environment
- GA-8. Ethical Practices:** Ability to apply ethical principles to engineering practices and professional responsibilities
- GA-9. Independent and Reflective Learning:** Ability to work as a member of a team, to plan and to integrate knowledge of various engineering disciplines and to lead teams in multidisciplinary settings
- GA-10. Communication:** Ability to make effective oral presentations and communicate technical ideas to a broad audience using written and oral means
- GA-11. Project Management and Finance:** Ability to lead and manage multidisciplinary teams by applying engineering and management principles
- GA-12. Life-long learning:** Ability to adapt to the changes and advancements in technology and engage in independent and life-long learning

17. Programme Outcomes (POs)

M.Tech. graduates will be able to:

- PO-1.** Acquire, comprehensive knowledge and understanding of the methodologies, principles, practices and technologies of the engineering domain to solve complex problems with technical competence
- PO-2.** Conceptualize, apply, analyze, synthesize and evaluate information related to complex engineering problems using principles of mathematics, science and engineering to create new and innovative solutions
- PO-3.** Provide solutions to engineering problems by designing systems, components or processes to meet the specified needs considering public health, safety, societal and the environmental considerations
- PO-4.** Review research literature, standards, guidelines, best practices, research methods and laboratory techniques to solve engineering problems through experimental investigations, analysis and interpretation of results
- PO-5.** Create, select and apply appropriate techniques and IT tools to model and solve complex engineering activities and utilize available resources effectively
- PO-6.** Understand the effect of engineering solutions on legal, cultural, social, public health and safety aspects and the consequent responsibilities

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Page 5 of 94
M.S. Ramaiah Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 054

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

- PO-7. Develop sustainable engineering solutions and assess their effect on society and environment
- PO-8. Understand and apply ethical principles to engineering practices and professional responsibilities
- PO-9. Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings
- PO-10. Make oral and written presentations to communicate technical ideas effectively to engineering community and society at large
- PO-11. Apply the knowledge of engineering and management principles to manage projects in multi-disciplinary environment with consideration to cost and time
- PO-12. Engage in lifelong learning and adapt to changing engineering/technology and societal requirements

18. Programme Goal

The programme goal is to produce graduates having critical, analytical and problem-solving skills, and ability to think independently, and to pursue a career in VLSI and Nanotechnology.

19. Program Educational Objectives (PEOs)

The objectives of the M.Tech.(VLSI and Nanotechnology) Programme are to:

- PEO-1. To provide in-depth knowledge in the specialized engineering domain to enable them to deliver efficient solutions for complex engineering problems by critical thinking
- PEO-2. To enable students to design and develop sustainable innovative solutions for industry and societal requirements through applied research by conducting engineering investigations through experimentation and usage of modern tools
- PEO-3. To inculcate ethics, communication, leadership, soft, managerial and entrepreneurial skills for a successful career in industries and to engage in lifelong learning



Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019

Page 6 of 94
Academic Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 054

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

20. Programme Specific Outcomes (PSOs)

At the end of the M.Tech.(VLSI and Nanotechnology) program, the graduate will be able to:

PSO-1. Apply the knowledge and principles of analog, digital and mixed signal circuits & nano-electronic devices, to conceptualize and provide efficient and customized solutions through critical analysis for electronic system development

PSO-2. Design and develop sustainable VLSI and Nanotechnology solutions to industry and societal requirements through applied research, concepts and techniques of FPGA Implementation, ASIC Design, Embedded Systems, SoCs, Quantum mechanics, Nanomaterials, involving simulation analysis and usage of modern EDA tools

PSO-3. Demonstrate ethics, leadership qualities, communication, entrepreneurial skills and involvement in lifelong learning for the betterment of organization, environment and society

21. Programme Structure:

Semester 1

Sl.No.	Code	Course Title	Theory (h/W/S)	Tutorials (h/W/S)	Practical (h/W/S)	Total Credits	Max. Marks
1	19VLC501A	Full Custom IC Design	3	0	2	4	100
2	19VLC502A	Quantum Mechanics and Nano Electronics	2	1	2	4	100
3	19VLC503A	Semi-Custom IC design	3	0	2	4	100
4	19VLC504A	Nano Scale Device Modelling and Simulation	2	1	2	4	100
5	19VLE5XXA	Refer to Elective Course Table	3	0	2	4	100
6	19FET508A	Research Methodology & IPR	2	--	--	2	50
7	19FET509A	Professional Communication	1	--	--	0	00
Total			16	2	10	22	550
Total number of contact hours per week			28 hours				
Number of credits can be registered			Minimum	18	Maximum	24	

Sl No	Code	Course Title	Theory (h/W/S)	Tutorials (h/W/S)	Practical (h/W/S)	Total Credits	Max. Marks
1	19VLC511A	FPGA System Design and Implementation	4	0	2	5	100
2	19VLC512A	Nano Materials and Devices	4	0	2	5	100
3	19VLE5XXA	Refer to Elective Course Table / MOOC	4	0	0	4	100
4	19VLE5XXA	Refer to Elective Course Table / MOOC	4	0	0	4	100



Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

5	19VLE5XXA	Refer to Elective Course Table / MOOC	4	0	0	4	100
6	19FET510A	Value Education	1			0	
Total			19	0	4	22	600
Total number of contact hours per week			23 hours				
Number of credits can be registered			Minimum	18	Maximum	24	

Semester 3

Sl.No.	Code	Course Title	Theory (h/W/S)	Tutorials (h/W/S)	Practical (h/W/S)	Total Credits	Max. Marks
1	19VLP521A	Internship/other activities			10	4	100
2	19VLP522A	Group project			15	8	200
3	19VLP523A	Dissertation and Publication (Phase 1)					
Total					25	12	300
Total number of contact hours per week			25 hours				

Semester 4

Sl.No.	Code	Course Title	Theory (h/W/S)	Tutorials (h/W/S)	Practical (h/W/S)	Total Credits	Max. Marks
1	19VLP523A	Dissertation and Publication (Phase 2)			24	24	400
Total					24	24	400
Total number of contact hours per week			24 hours				

Elective Course List				
Stream / Specialization	Sl. No.	Course Code	Course Title	Course Category
VLSI	E11	19VLE511A	Signal Integrity and High-Speed Design	A
	E12	19VLE512A	VLSI Verification and Testing	B
	E13	19VLE513A	Analog and Mixed Signal Circuit Design	B
	E14	19VLE514A	Programmable Embedded SoCs	B
Nanotechnology	E21	19VLE521A	Sensors and Systems Design	A
	E22	19VLE522A	MEMS and NEMS	B
	E23	19VLE523A	Advanced Nano Materials and Applications	B
	E24	19VLE524A	Quantum Computing and Communication	B

Note:

The Vacations and other activities shall be as per the Timetable for the corresponding batch.

22. Course Delivery: As per the Timetable

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Academic Registrar
M.S. Ramaiah University of Applied Sciences
Page 8 of 94

Handwritten signature

23. Teaching and Learning Methods

1. Face to Face Lectures using Audio-Visuals
2. Workshops, Group Discussions, Debates, Presentations
3. Demonstrations
4. Guest Lectures
5. Laboratory work/Field work/Workshop
6. Industry Visit
7. Seminars
8. Group Exercises
9. Project Work
10. Project
11. Exhibitions
12. Technical Festivals

24. Assessment and Grading

24.1. Components of Grading

There shall be **two components** of grading in the assessment of each course:

Component 1, Continuous Evaluation (CE): This component involves multiple subcomponents (SC1, SC2, etc.) of learning assessment. The assessment of the subcomponents of CE is conducted during the semester at regular intervals. This subcomponent represents the formative assessment of students' learning.

Component 2, Semester-end Examination (SEE): This component represents the summative assessment carried out in the form an examination conducted at the end of the semester. Marks obtained CE and SEE components have equal weightage (CE: 50% and SEE: 50%) in determining the final marks obtained by a student in a Course. The complete details of Grading are given in the Academic Regulations.

24.2. Continuous Evaluation Policies

Continuous evaluation depends on the type of the course as discussed below:

24.2.1 Theory Courses

The following **TWO options** are available for each Faculty to perform the CE exercise.

Option 1 for a Theory Course:

Theory Course			
SC1	SC2	SC3	SC4
25 Marks	25 Marks	25 Marks	25 Marks

In, Option 1, there shall be four subcomponents of CE (SC1, SC2, SC3 and SC4). Each subcomponent is evaluated individually for 25 marks. It is mandatory that two of the four subcomponents are term-tests. The remaining two subcomponents can be of any of the following types:



Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

- a) Online Test
- b) Assignments/Problem Solving
- c) Field Assignment
- d) Open Book Test
- e) Portfolio
- f) Reports
- g) Case Study
- h) Group Task
- i) Any other

After the four subcomponents are evaluated, the CE component marks are determined as:

$$\text{CE Component Marks} = (\text{Total of the marks obtained in all the four subcomponents}) \div 2$$

An additional subcomponent (SC5) may be used at the discretion of the Faculty/Department. The department can conduct the 5th subcomponent SC5 if this subcomponent gives benefit to students. If the Department/Faculty conducts the SC5 subcomponent of evaluation, and the score obtained by the student in SC5 is greater than the lowest score of the previous four subcomponents SC1 to SC4, then it replaces the lowest of the four scores.

Option 2 for a Theory Course:

Theory Course			
SC1	SC2	SC3	SC4
25 Marks	25 Marks	25 Marks	25 Marks

In Option 2, there shall be four subcomponents, each carrying 25 marks. Out of these, there shall be two assignments and two term-tests. The assignments can be of any of the following types:

- a) Online Test
- b) Problem Solving
- c) Field Assignment
- d) Open Book Test
- e) Portfolio
- f) Reports
- g) Case Study
- h) Group Task
- i) Any other

After the four subcomponents of CE are evaluated, the CE component Marks are determined as:

$$\text{CE Component Marks} = (\text{Best of two Assignment Marks}) + (\text{Best of two Term-Test Marks})$$

Each Faculty Dean, in consultation with the heads of all departments in the Faculty and the Faculty Academic Registrar, decides whether Option 1 or Option 2 is adopted for each programme offered by the Faculty. He/she notifies the students about the option at the beginning of the semester.



Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

24.2.2 Laboratory Course

For a laboratory course, the scheme for determining the CE marks is as under:

Laboratory Course		
SC1	SC2	SC3 (Optional)
25 Marks	25 Marks	25 Marks

The subcomponents can be of any of the following types:

- Laboratory / Clinical Work Record
- Experiments
- Computer Simulations
- Creative Submission
- Virtual Labs
- Viva / Oral Exam
- Lab Manual Report
- Any other (e.g. combinations)

After the subcomponents of CE are evaluated, the CE component Marks are determined as:

$$\text{CE Component Marks} = (\text{Total of the best two subcomponent marks out of the three}) \div 2$$

24.2.3 Course Having a Combination of Theory and Laboratory

For a course that contains the combination of theory and laboratory sessions, the scheme for determining the CE marks is as under:

For a Course having a Combination of Theory and Laboratory Sessions			
SC1 (Theory)	SC2 (Theory)	SC3 (Theory)	SC4 (Laboratory)
25 Marks	25 Marks	25 Marks	25 Marks

There shall be four subcomponents, each carrying 25 marks. Out of these, there shall be two term-tests and an assignment to evaluate the students' performance in theory. The fourth subcomponent shall be set to evaluate the students' performance in the laboratory.

The theory assignment can be of any of the following types:

- Online Test
- Problem Solving
- Field Assignment
- Open Book Test
- Portfolio
- Reports



Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

- g) Case Study
- h) Group Task
- i) Any other

The laboratory subcomponent can be of any of the following types:

- a) Laboratory / Clinical Work Record
- b) Experiments
- c) Computer Simulations
- d) Creative Submission
- e) Virtual Labs
- f) Viva / Oral Exam
- g) Lab Manual Report
- h) Any other (e.g. combinations)

After the four subcomponents are evaluated, the CE component marks are determined as:

CE Component Marks = (Total of the marks obtained in all the four subcomponents) ÷ 2

25. Student Support for Learning

1. Course Notes
2. Reference Books in the Library
3. Magazines and Journals
4. Internet Facility
5. Computing Facility
6. Laboratory Facility
7. Workshop Facility
8. Staff Support
9. Lounges for Discussions
10. Any other support that enhances their learning

26. Quality Control Measures

1. Review of Course Notes
2. Review of Question Papers and Assignment Questions
3. Student Feedback
4. Moderation of Assessed Work
5. Opportunities for students to see their assessed work
6. Review by external examiners and external examiners reports
7. Staff Student Consultative Committee meetings
8. Student exit feedback
9. Subject Assessment Board (SAB)
10. Programme Assessment Board (PAB)



Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019

Academic Registrar
Page 12 of 94
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 054

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

27. Programme Map (Course-PO-PSO Map)

Sem.	Course Title	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PO-7	PO-8	PO-9	PO-10	PO-11	PO-12	PSO-1	PSO-2	PSO-3
1	Full Custom IC Design	3	3	3	2	3	2	1	2	1	3		1	3	3	3
1	Quantum Mechanics and Nano Electronics	3	3	3	2	2	2	1	2	1	3		1	3	2	3
1	Semi-Custom IC design	3	3	3	2	3	2	1	2	1	3		1	3	3	3
1	Nano Scale Device Modelling and Simulation	3	3	3	1	1	2	1	2	1	3		1	3	2	3
1	Signal Integrity and High-Speed Design	3	3	3	2	2	2	1	2	1	3		1	3	2	3
1	Sensors and Systems Design	3	3	3	1	1	2	1	2	1	3		1	3	2	3
1	Research Methodology & IPR	2	2	1	2				2		3	1	1	2	2	3
1	Professional Communication	1							2		3		1	1		3
2	FPGA System Design and Implementation	3	3	3	2	3	2	1	2	1	3		1	3	3	3
2	Nano Materials and Devices	3	3	3	1	1	2	1	2	1	3		1	3	2	3
2	VLSI Verification and Testing	3	3	3	1	1	2	1	2	1	3		1	3	2	3
2	Analog and Mixed Signal Circuit Design	3	3	3	1	1	2	1	2	1	3		1	3	2	3
2	Programmable Embedded SoCs	3	3	3	1		2	1	2	1	3		1	3	2	3
2	MEMS and NEMS	3	3	3	1		2	1	2	1	3		1	3	2	3
2	Advanced Nano Materials and Applications	3	3	3	1		2	1	2	1	3		1	3	2	3
2	Quantum Computing and Communication	3	3	3	1		2	1	2	1	3		1	3	2	3
2	Value Education							3	3		2				3	3
3	Internship/other activities	3	3	3	3	3	2	1	2	1	3	1	1	3	3	3
3	Group project	3	3	3	3	3	2	1	2	1	3	3	1	3	3	3
4	Dissertation and Publication	3	3	3	3	3	2	1	2	1	3	2	1	3	3	3

28. Co-curricular Activities

Students are encouraged to take part in co-curricular activities like seminars, conferences, symposia, paper writing, attending industry exhibitions, project competitions and related activities for enhancing their knowledge and networking.

29. Cultural and Literary Activities

Annual cultural festivals are held to showcase the creative talents in students. They are involved in planning and organizing the activities.

30. Sports and Athletics

Students are encouraged to take part in sports and athletic events regularly. Annual sports meet will be held to demonstrate sportsmanship and competitive spirit.



Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

Course Specifications: Signal Integrity and High-Speed Design

Course Title	Signal Integrity and High-Speed Design
Course Code	19VLE511A
Course Type	Professional Core Elective
Department	Electronics and Communication Engineering
Faculty	Engineering and Technology

1. Course Summary

This course deals with design, create, capture, simulation and implementation of the high-speed interconnects and printed circuit board design. The course deals with high frequency signal propagation issues such as crosstalk, reflections, ringing, SSN, SSO, ground/power bounce and EMI. Analysis, simulation and implementation of various techniques such as termination techniques, crosstalk avoidance and topological design of nets to achieve better signal integrity are emphasized. Students will be trained on the PCB design and simulation.

2. Course Size and Credits:

Number of Credits	04
Credit Structure (Lecture: Tutorial: Practical)	3:0:2
Total Hours of Interaction	75
Number of Weeks in a Semester	15
Department Responsible	Electronics and Communication Engineering
Total Course Marks	100
Pass Criterion	As per the Academic Regulations
Attendance Requirement	As per the Academic Regulations

3. Course Outcomes (COs)

After the successful completion of this course, the student will be able to:

- CO 1. Discuss the concepts of high-speed interconnects and Printed Circuit Board (PCB)
- CO 2. Analyze and solve signal integrity issues in terms of crosstalk, SSN, signal return path, ground bounce, differential signaling, EMI and integration issues of PCB
- CO 3. Identify and apply appropriate design optimization to overcome signal integrity issues
- CO 4. Develop components library and arrive at schematic for a given design
- CO 5. Design, create, capture and develop a layout for the schematic and perform component placement, and routing to realize PCB for a given application
- CO 6. Use standard software tools to implement and analyze reflection, crosstalk and EMI for high speed PCB

4. Course Contents

Unit 1 (Introduction to PCB Design): PCB Design Environment, History of PCB, Major types of PCBs, Parts of PCB, Various Chip packages, multilayer PCB, Challenges in Modern PCBs, Importance of Interconnect design, Issues in high speed boards, Frequency, Time and Distance, Lumped and Distributed Systems, Four Kinds of Reactance, Ordinary , Mutual Capacitance and Inductance, Inductive and Capacitive coupling.

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Academic Registrar
M.S. Ramaiah University of Applied Sciences
Page 14 of 94

A handwritten signature in blue ink, appearing to be 'K. S. Ramaiah', is written over the printed name of the Academic Registrar.

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

Unit 2 (Signal Integrity and its Components): Microstrip and Stripline, Transmission lines types - Lumped, Distributed, Odd and Even; Reflection calculations, Signal integrity, Effect of signal integrity on Transmission Line and Reflection Issues, Near-end and Far-end Crosstalk, Crosstalk Induced Noise, Effect of crosstalk on transmission line parameters, Termination techniques to reduce crosstalk, Design Guidelines, Crosstalk simulation and analysis, Effect of Crosstalk, Termination Techniques.

Unit 3 (Routing and its attributes): Routing topologies, Rise and fall time degradation, Signal Skew, Termination techniques and reflection analysis, PCB Stack up and Return Path Discontinuities, Power rule, power supply for board, Power distribution network and de-coupling capacitor, Ground/Power Bounce, Design of Decoupling Capacitor, IR drop analysis

Unit 4 (IBIS Models and EMI): IBIS Models and their use, Analysis of Signal Integrity, Modeling and Simulation, Definitions, Impact of EMI and EMC, Radiation and Conduction, Types of EMI, EMI characterization, EMI Suppression, Bypassing & Decoupling, Grounding techniques & Trace Routing to avoid interference, EMI simulation and Analysis, ESD Protection

Unit 5 (Fabrication of PCB): Materials used in FPCB, Direct and Indirect Materials, Manufacturing Processes for a Multi-layer PCB, Inner Layer Processing, Material Selection, Laminating and Imaging of Internal Layers, Etch Process, Completed Inner Layer Core, Electro-plating, Design for Manufacturability (DFM), IPC Standard (2221-General): Material Consideration and Documentation, Electrical consideration of PCB design.

5. Course Map (CO-PO-PSO Map)

	Programme Outcomes (POs)												Programme Specific Outcomes (PSOs)		
	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PO-7	PO-8	PO-9	PO-10	PO-11	PO-12	PSO-1	PSO-2	PSO-3
CO-1	3								1			1	3		1
CO-2	3								1			1	3		1
CO-3	1	3	3	2	3				1			1	3	3	1
CO-4	1	3	3	2	3	2	1	2	1	3		1	3	3	3
CO-5	1	2	2	2	1	2	1	2	1	2		1	2	2	1
CO-6					3	1				3		1		3	3

3: Very Strong Contribution, 2: Strong Contribution, 1: Moderate Contribution

6. Course Teaching and Learning Methods

Teaching and Learning Methods	Duration in hours	Total Duration in Hours
Face to Face Lectures		40
Demonstrations		05
1. Demonstration using Videos	05	
2. Demonstration using Physical Models / Systems	00	
3. Demonstration on a Computer	00	
Numeracy		00
1. Solving Numerical Problems	00	
Practical Work		30
1. Course Laboratory	30	

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Academic Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 054

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

2. Computer Laboratory	00	
3. Engineering Workshop / Course/Workshop / Kitchen	00	
4. Clinical Laboratory	00	
5. Hospital	00	
6. Model Studio	00	
Others		
1. Case Study Presentation	00	00
2. Guest Lecture	00	
3. Industry / Field Visit	00	
4. Brain Storming Sessions	00	
5. Group Discussions	00	
6. Discussing Possible Innovations	00	
Term Tests, Laboratory Examination/Written Examination, Presentations		10
Total Duration in Hours		85

7. Course Assessment and Reassessment

The details of the components and subcomponents of course assessment are presented in the Programme Specifications document pertaining to the M.Tech. (VLSI and Nanotechnology) Programme. The procedure to determine the final course marks is also presented in the Programme Specifications document.

The evaluation questions are set to measure the attainment of the Cos. In either component (CE or SEE) or subcomponent of CE (SC1, SC2, SC3 or SC4), Cos are assessed as illustrated in the following Table.

Focus of Cos on each Component or Subcomponent of Evaluation					
Subcomponent ▶	Component 1: CE (50% Weightage)				Component 2: SEE (50% Weightage)
	SC1	SC2	SC3	SC4	
Subcomponent Type ▶	Term Test	Assignment	Term Test	Assignment	100 Marks
Maximum Marks ▶	25	25	25	25	
CO-1	X				X
CO-2	X		X		X
CO-3		X	X	X	X
CO-4		X		X	
CO-5		X		X	
CO-6		X		X	

The details of SC1, SC2, SC3 or SC4 are presented in the Programme Specifications Document.

The Course Leader assigned to the course, in consultation with the Head of the Department, shall provide the focus of COs in each component of assessment in the above template at the beginning of the semester.

Course reassessment policies are presented in the Academic Regulations document.

8. Achieving COs

The following skills are directly or indirectly imparted to the students in the following teaching and learning methods:



Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

S. No	Curriculum and Capabilities Skills	How imparted during the course
1.	Knowledge	Classroom Lectures
2.	Understanding	Classroom Lectures, Self-study
3.	Critical Skills	Assignment
4.	Analytical Skills	Assignment
5.	Problem Solving Skills	Assignment and Exam
6.	Practical Skills	Assignment
7.	Group Work	Assignment
8.	Self-Learning	Self-learning
9.	Written Communication Skills	Assignment
10.	Verbal Communication Skills	--
11.	Presentation Skills	Assignment
12.	Behavioral Skills	--
13.	Information Management	Assignment
14.	Personal Management	--
15.	Leadership Skills	--

9. Course Resources

a. Essential Reading

1. Course Notes
2. Howard. W. Johnson and Martin Graham (2004). High Speed Digital Design, A Handbook of Black Magic.
3. 2. Douglas Brooks (2003). Signal Integrity Issues and Printed Circuit Board Design, Prentice Hall

b. Recommended Reading

1. Mark I. Montrose (2004). Printed Circuit Board Design Techniques for EMC Compliance: A Handbook for Designers, IEEE Press.
2. Eric Bogatin (2004). Signal Integrity-Simplified, Prentice Hall.

c. Website

1. <http://nptel.ac.in/>

10. Course Organization

Course Code	19VLE511A	
Course Title	Signal Integrity and High-Speed Design	
Course Leader's Name	As per Timetable	
Course Leader's Contact Details	Phone:	080-49065555
	E-mail:	hod.ec.et@msruas.ac.in
Course Specifications Approval Date	09-July-2019	
Next Course Specifications Review Date	July-2021	

Dean
Faculty of Engineering & Technology
M.S. Ramalah University of Applied Sciences
Bangalore - 560 058.

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Academic Registrar
Page 17 of 94
M.S. Ramalah University of Applied Sciences
Bangalore - 560 054

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

Course Specifications: Sensors and Systems Design

Course Title	Sensors and Systems Design
Course Code	19VLE521A
Course Type	Professional Core Elective
Department	Electronics and Communication Engineering
Faculty	Engineering and Technology

1. Course Summary

The course deals with theoretical understanding of various physical phenomena behind the operation of different types of sensors, designing appropriate electronic interface to develop a complete sensor system. Sensors such as magnetic, optical, bio, chemical, radiation, electrical and mechanical are focused here. Students are introduced to Nano sensors for physical, chemical and biological applications. The course also emphasis on fabricating sensors and electronic interfaces on an integrated circuit.

2. Course Size and Credits:

Number of Credits	04
Credit Structure (Lecture: Tutorial: Practical)	3:0:2
Total Hours of Interaction	75
Number of Weeks in a Semester	15
Department Responsible	Electronics and Communication Engineering
Total Course Marks	100
Pass Criterion	As per the Academic Regulations
Attendance Requirement	As per the Academic Regulations

3. Course Outcomes (COs)

After the successful completion of this course, the student will be able to:

- CO 1. Choose and discuss the working principle of sensors for various applications
- CO 2. Design electronic interface circuits for reading data from sensors
- CO 3. Analyze various methods /steps in the fabrication of Nano sensors
- CO 4. Design high performance data converters suitable for sensor-based systems
- CO 5. Apply the concepts of sensors and signal processing to design a sensor-based data acquisition system
- CO 6. Design, develop and simulate a sensor-based system

4. Course Contents

Unit 1 (Introduction to Sensor System): Sensors, Signals and Systems, Units of Measurements, Sensor Characteristics, Different types of sensors, comparison between analog and digital sensors, specification and working principles of analog sensors, specifications and working principles of digital sensors, case study.

Unit 2 (Electrical Characteristics of Sensors): Electric Charges, Fields, and Potentials; Capacitance; Magnetism; Induction; Resistance; Piezoelectric Effect; Hall Effect; Temperature and Thermal Properties of Material; Heat Transfer; Light; Dynamic Models of Sensor Elements.



Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

Unit 3 (Characteristics of Interfacing Circuits): Input Characteristics of Interface Circuits, Amplifiers, Excitation Circuits, Analog to Digital Converters, Direct Digitization and Processing, Bridge Circuits, Data Transmission, Batteries for Low Power Sensors.

Unit 4 (Types of Sensors): Motion Detectors; Position, Displacement, Force, Strain, and Tactile Sensors, Pressure Sensors, Temperature Sensors, Nano sensors –Advantages- Nano sensors -physical, chemical and biological applications.

Unit 5 (Materials and Fabrication of Sensors): Materials- surface processing -Deposition of Thin and Thick Films-Spin-Casting- Vacuum Deposition- Sputtering- Chemical Vapor Deposition. Nano technology- Photolithography - Silicon Micromachining.

5. Course Map (CO-PO-PSO Map)

	Programme Outcomes (POs)												Programme Specific Outcomes (PSOs)		
	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PO-7	PO-8	PO-9	PO-10	PO-11	PO-12	PSO-1	PSO-2	PSO-3
CO-1	3								1			1	3		1
CO-2	3								1			1	3		1
CO-3	1	3	3	2	3				1			1	3	3	1
CO-4	1	3	3	2	3	2	1	2	1	3		1	3	3	3
CO-5	1	2	2	2	1	2	1	2	1	2		1	2	2	1
CO-6	1	1	2	2	3	2	1			3		1	2	3	3

3: Very Strong Contribution, 2: Strong Contribution, 1: Moderate Contribution

6. Course Teaching and Learning Methods

Teaching and Learning Methods	Duration in hours	Total Duration in Hours
Face to Face Lectures		40
Demonstrations		05
1. Demonstration using Videos	05	
2. Demonstration using Physical Models / Systems	00	
3. Demonstration on a Computer	00	
Numeracy		00
1. Solving Numerical Problems	00	
Practical Work		30
1. Course Laboratory	30	
2. Computer Laboratory	00	
3. Engineering Workshop / Course/Workshop / Kitchen	00	
4. Clinical Laboratory	00	
5. Hospital	00	
6. Model Studio	00	
Others		00
1. Case Study Presentation	00	
2. Guest Lecture	00	
3. Industry / Field Visit	00	



Academic Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 054

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

4. Brain Storming Sessions	00	
5. Group Discussions	00	
6. Discussing Possible Innovations	00	
Term Tests, Laboratory Examination/Written Examination, Presentations		10
Total Duration in Hours		85

7. Course Assessment and Reassessment

The details of the components and subcomponents of course assessment are presented in the Programme Specifications document pertaining to the M.Tech. (VLSI and Nanotechnology) Programme. The procedure to determine the final course marks is also presented in the Programme Specifications document.

The evaluation questions are set to measure the attainment of the COs. In either component (CE or SEE) or subcomponent of CE (SC1, SC2, SC3 or SC4), Cos are assessed as illustrated in the following Table.

Focus of Cos on each Component or Subcomponent of Evaluation					
Subcomponent ▶	Component 1: CE (50% Weightage)				Component 2: SEE (50% Weightage)
	SC1	SC2	SC3	SC4	
Subcomponent Type ▶	Term Test	Assignment	Term Test	Assignment	100 Marks
Maximum Marks ▶	25	25	25	25	
CO-1	X				X
CO-2	X		X		X
CO-3		X	X	X	X
CO-4		X		X	
CO-5		X		X	
CO-6		X		X	

The details of SC1, SC2, SC3 or SC4 are presented in the Programme Specifications Document.

The Course Leader assigned to the course, in consultation with the Head of the Department, shall provide the focus of COs in each component of assessment in the above template at the beginning of the semester.

Course reassessment policies are presented in the Academic Regulations document.

8. Achieving COs

The following skills are directly or indirectly imparted to the students in the following teaching and learning methods:

S. No	Curriculum and Capabilities Skills	How imparted during the course
1.	Knowledge	Classroom Lectures
2.	Understanding	Classroom Lectures, Self-study
3.	Critical Skills	Assignment
4.	Analytical Skills	Assignment
5.	Problem Solving Skills	Assignment and Exam
6.	Practical Skills	Assignment
7.	Group Work	Assignment
8.	Self-Learning	Self-learning
9.	Written Communication Skills	Assignment
10.	Verbal Communication Skills	--



Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

11.	Presentation Skills	Assignment
12.	Behavioral Skills	--
13.	Information Management	Assignment
14.	Personal Management	--
15.	Leadership Skills	--

9. Course Resources

a. Essential Reading

1. Course Notes
2. J. Fraden (2006), Handbook of Modern Sensors: Physical, Designs, and Applications, AIP Press, Springer.
3. D. Patranabis (2013), Sensors and Transducers, PHI Publication, New Delhi.

b. Recommended Reading

1. S. M. Sze (1994), Semiconductor Sensors, Wiley-Interscience.
2. Vinod Kumar Khanna (2011), Nanosensors: Physical, Chemical, and Biological, 1st Edition, CRC Press

c. Website

1. <http://nptel.ac.in/>

10. Course Organization

Course Code	19VLE521A	
Course Title	Sensors and Systems Design	
Course Leader's Name	As per Timetable	
Course Leader's Contact Details	Phone:	080-49065555
	E-mail:	hod.ec.et@msruas.ac.in
Course Specifications Approval Date	09-July-2019	
Next Course Specifications Review Date	July-2021	

Dean
Faculty of Engineering & Technology
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 058.

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Academic Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 054

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

Course Specifications: Research Methodology and IPR

Course Title	Research Methodology and IPR
Course Code	19FET508A
Course Type	Ability Enhancement Compulsory
Department	Electronics and Communication Engineering
Faculty	Engineering and Technology

1. Course Summary

This course deals with the principles of research, research methodology, significant phases of research, Intellectual property and its rights. Students are taught the realistic guidelines to be followed in the choice of field of research, topic of research and formulation of research problem. Key and careful considerations in the choice of tools for the solution of research problem are covered in this module. The module emphasizes the desirable close knit relation between innovation and concept of out of the box thinking. The principles of effective research and the need for a Proactive approach in a successful research programme are also explained. The course discusses the significant role of Literature Review in a research cycle and the expectations from good literature review as well as procedure for systematic literature review. This course gives insight of the intellectual property rights and over view of the benefits.

2. Course Size and Credits:

Number of Credits	02
Credit Structure (Lecture: Tutorial: Practical)	2:0:0
Total Hours of Interaction	30
Number of Weeks in a Semester	15
Department Responsible	Electronics and Communication Engineering
Total Course Marks	50
Pass Criterion	As per the Academic Regulations
Attendance Requirement	As per the Academic Regulations

3. Course Outcomes (COs)

After the successful completion of this course, the student will be able to:

- CO-1. Describe the value, scope, relevance and mandatory steps of research as well as principles of effective research, Nature of Intellectual Property.
- CO-2. Discuss the guidelines to progress from the choice of broad field of research to specific topic of research, patent rights, process of patenting at National and International level, New Developments in IPR.
- CO-3. Demonstrate the application and utility of the Systematic approach and out of box thinking concepts for research to be effective.
- CO-4. Adapt, analyze and prepare well-structured research proposal and research paper invoking clearly outlined principles.



Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

4. Course Contents

Unit 1 (Foundations of Research): Definitions of Research, Mandatory Steps in Research, Types of Research, Relevance of Research for Innovation and Technology Development, Effective Research and Self Discipline.

Unit 2 (Formulation of Research Problem): Identification of problems, Narrowing down the problem, Factors to be considered for problem selection. History and Evolution of Science & Technology.

Unit 3 (Out of the Box Thinking and Systematic Approach in Research): Transformation to Impossible Thinking, Convergent and Divergent Thinking, Generation, Evaluation and Selection of Ideas, Critical Thinking

Literature Review – Importance of Literature Review, Constituents of Good Literature Review, Strategies for Literature Search, Referencing, Paraphrasing, and Summarizing Academic Standards and Ethics

Research Proposal – Structure of a Good Research Proposal, Getting Started, Tips for Compilation of Good Research Proposal.

Unit 4 (Nature of Intellectual Property): Patents, Designs, Trade and Copyright.

Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

Unit 5: (Patent Rights): Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases, Geographical Indicators.

Unit 6: (New Developments in IPR): Administration of Patent System. New developments in IPR; IPR of Biological Systems, Copy rights for Software. Traditional knowledge Case Studies.

5. Course Map (CO-PO-PSO Map)

	Programme Outcomes (POs)												Programme Specific Outcomes (PSOs)		
	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PO-7	PO-8	PO-9	PO-10	PO-11	PO-12	PSO-1	PSO-2	PSO-3
CO-1				3		3		3	2	3	2	1	0	3	3
CO-2				3		3		3		1	1	1	0	3	3
CO-3				3		3	3	3		1		1	0	3	3
CO-4				3				2		3	3	1	0	3	3

3: Very Strong Contribution, 2: Strong Contribution, 1: Moderate Contribution

6. Course Teaching and Learning Methods

Teaching and Learning Methods	Duration in hours	Total Duration in Hours
Face to Face Lectures		20
Demonstrations		00
1. Demonstration using Videos	00	
2. Demonstration using Physical Models / Systems	00	
3. Demonstration on a Computer	00	
Numeracy		00

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Academic Registrar
Page 23 of 94
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 054

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

1. Solving Numerical Problems	00	
Practical Work		
1. Course Laboratory	00	00
2. Computer Laboratory	00	
3. Engineering Workshop / Course/Workshop / Kitchen	00	
4. Clinical Laboratory	00	
5. Hospital	00	
6. Model Studio	00	
Others		
1. Case Study Presentation	06	10
2. Guest Lecture	04	
3. Industry / Field Visit	00	
4. Brain Storming Sessions	00	
5. Group Discussions	00	
6. Discussing Possible Innovations	00	
Term Tests, Laboratory Examination/Written Examination, Presentations		10
Total Duration in Hours		40

7. Course Assessment and Reassessment

The details of the components and subcomponents of course assessment are presented in the Programme Specifications document pertaining to the B.Tech. (Electronics and Communication Engineering) Programme. The procedure to determine the final course marks is also presented in the Programme Specifications document.

The evaluation questions are set to measure the attainment of the COs. In either component (CE or SEE) or subcomponent of CE (SC1, SC2, SC3 or SC4), COs are assessed as illustrated in the following Table.

Focus of COs on each Component or Subcomponent of Evaluation			
Subcomponent ▶	Component 1: CE (50% Weightage)		Component 2: SEE (50% Weightage)
	SC1	SC2	
Subcomponent Type ▶	Term Test	Assignment	50 Marks
Maximum Marks ▶	25	25	
CO-1	☐	☐	☐
CO-2	☐	☐	☐
CO-3	☐	☐	☐
CO-4		☐	

The details of SC1, SC2, SC3 or SC4 are presented in the Programme Specifications Document.

The Course Leader assigned to the course, in consultation with the Head of the Department, shall provide the focus of COs in each component of assessment in the above template at the beginning of the semester. Course reassessment policies are presented in the Academic Regulations document.

8. Achieving COs

The following skills are directly or indirectly imparted to the students in the following teaching and learning methods:



Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

S. No	Curriculum and Capabilities Skills	How imparted during the course
1.	Knowledge	Classroom lectures
2.	Understanding	Classroom lectures, Self-study
3.	Critical Skills	Assignment
4.	Analytical Skills	Assignment
5.	Problem Solving Skills	Assignment, Examination
6.	Practical Skills	Assignment
7.	Group Work	--
8.	Self-Learning	Self-study
9.	Written Communication Skills	Assignment, Examination
10.	Verbal Communication Skills	--
11.	Presentation Skills	--
12.	Behavioral Skills	--
13.	Information Management	Assignment
14.	Personal Management	--
15.	Leadership Skills	--

9. Course Resources

a. Essential Reading

1. Course notes
2. Melville, S. and Goddard, W. (1996) Research Methodology: An Introduction for Science & Engineering Students, Juta
3. Merges, R. P., Menell, P. S. and Lemley, M. A. (2016) Intellectual Property in New Technological Age, Fourth Edition, Wolters Kluwer

b. Recommended Reading

1. Kothari, C. R. and Garg G. (2019) Research Methodology: Methods and Techniques, New Age International Publishers

c. Other Electronic Resources

1. NPTEL Videos and Digital Library

10. Course Organization

Course Code	20FET508A		
Course Title	Research Methodology and IPR		
Course Leader's Name	As per Timetable		
Course Leader's Contact Details	Phone:	+91-80-4906-5555	
	E-mail:	hod.aae.et@msruas.ac.in	
Course Specifications Approval Date	9-July-2019		
Next Course Specifications Review Date	July-2021		

Dean
Faculty of Engineering & Technology
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 058.

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Academic Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 054

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

Course Specifications: Professional Communication

Course Title	Professional Communication
Course Code	19FET509A
Course Type	Ability Enhancement Compulsory
Department	Electronics and Communication Engineering
Faculty	Engineering and Technology

1. Course Summary

This course aims at sensitising students to the essentials of professional communication. Professional Communication is essential to achieve the objectives of an organisation.

2. Course Size and Credits:

Number of Credits	00
Credit Structure (Lecture: Tutorial: Practical)	0:0:0
Total Hours of Interaction	15
Number of Weeks in a Semester	15
Department Responsible	Directorate of Transferable Skills and Leadership Development
Total Course Marks	25
Pass Criterion	As per the Academic Regulations
Attendance Requirement	As per the Academic Regulations

3. Course Outcomes (COs)

After the successful completion of this course, the student will be able to:

- CO-1. Compose effective written business communication
- CO-2. Practice the techniques of presentation

4. Course Contents

Unit 1 (Communication - Introduction): Introduction to Professional Communication, Conversation and Listening

Unit 2 (Communication – Reading Skills): Reading Skills for Effective Professional Communication:
Introduction, SQ3R (Survey, Question, Read, Retrieve, and Review) Technique of Reading

Unit 3 (Communication - Writing Skills): Written Business Communication: Writing Memos, Letters, Circulars and Notices, Communicating through Email

Unit 4 (Communication - Presentation): Presentation Skills: Message development, content, projection, inflection, and delivery



Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

5. Course Map (CO-PO-PSO Map)

	Programme Outcomes (POs)												Programme Specific Outcomes (PSOs)		
	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PO-7	PO-8	PO-9	PO-10	PO-11	PO-12	PSO-1	PSO-2	PSO-3
CO-1					2					2				2	2
CO-2										3					3
3: Very Strong Contribution, 2: Strong Contribution, 1: Moderate Contribution															

6. Course Teaching and Learning Methods

Teaching and Learning Methods	Duration in hours	Total Duration in Hours
Face to Face Lectures		09
Demonstrations		0
1. Demonstration using Videos	00	
2. Demonstration using Physical Models / Systems	00	
3. Demonstration on a Computer	00	
Numeracy		0
1. Solving Numerical Problems	00	
Practical Work		
1. Course Laboratory	00	
2. Computer Laboratory	00	
3. Engineering Workshop / Course/Workshop / Kitchen	00	
4. Clinical Laboratory	00	
5. Hospital	00	
6. Model Studio	00	
Others		06
1. Case Study Presentation	02	
2. Guest Lecture	00	
3. Industry / Field Visit	00	
4. Brain Storming Sessions	00	
5. Group Discussions	04	
6. Discussing Possible Innovations	00	
In-class assessments, Term Tests, Laboratory Examination/Written Examination, Presentations		3
Total Duration in Hours		18

7. Course Assessment and Reassessment

The details of the components and subcomponents of course assessment are presented in the Programme Specifications document pertaining to the M.Tech. Programme. The procedure to determine the final course marks is also presented in the Programme Specifications document.

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Academic Registrar
Page 27 of 94
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 054

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

The evaluation questions are set to measure the attainment of the COs. In either component (CE or SEE) or subcomponent of CE (SC1, SC2, SC3 or SC4), COs are assessed as illustrated in the following Table.

Focus of CO's on each Component or Subcomponent of Evaluation:

	Component 1: CE (100% Weightage)	Component 2: SEE (0% Weightage)
Subcomponent ▶ <input type="checkbox"/>	SC1	0 Marks
Subcomponent Type ▶ <input type="checkbox"/>	In-Class Assessment	
Maximum Marks ▶ <input type="checkbox"/>	25	
CO-1	X	
CO-2	X	

The Course Leader assigned to the course, in consultation with the Head of the Department, shall provide the focus of COs in each component of assessment in the above template at the beginning of the semester.

Course reassessment policies are presented in the Academic Regulations document.

8. Achieving COs

The following skills are directly or indirectly imparted to the students in the following teaching and learning methods:

S. No	Curriculum and Capabilities Skills	How imparted during the course
1.	Knowledge	Face to face lectures
2.	Understanding	Face to face lectures, group discussions
3.	Critical Skills	--
4.	Analytical Skills	Face to face lectures, activities, , group discussions, assignment
5.	Problem Solving Skills	--
6.	Practical Skills	Face to face lectures, activities, , group discussions, course work
7.	Group Work	Course work, practice, assignment, group discussion
8.	Self-Learning	Course work, practice, assignment, group discussion
9.	Written Communication Skills	Face to face lectures, Course work, practice, assignment, group discussion
10.	Verbal Communication Skills	Face to face lectures, Course work, practice, assignment, group discussion
11.	Presentation Skills	--
12.	Behavioral Skills	Course work, practice, assignment, group discussion, presentation practice, role plays
13.	Information Management	Assignment
14.	Personal Management	--



Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

15.	Leadership Skills	--
-----	-------------------	----

9. Course Resources

a. Essential Reading

1. Class Notes
2. Dr. C.S.G. Krishnamacharyulu (2016) Business Communication, Himalaya Publishing House

b. Recommended Reading

1. V. Lesikar, John D. Pettit, Jr., Marie E. Flatley. (1999), Basic Business Communication, 8th Edition, Tata McGraw Hill

c. Magazines and Journals

d. Websites

www.myenglishpages.com

e. Other Electronic Resources

1. Electronic resources on the course area are available on RUAS library

10. Course Organization

Course Code	19FET509A	
Course Title	Professional Communication	
Course Leader's Name	As per Timetable	
Course Leader's Contact Details	Phone:	+91-80-453666666
	E-mail:	director.tsld@msruas.ac.in
Course Specifications Approval Date	24-JULY-2019	
Next Course Specifications Review Date	MAY-2021	

□ □ □

Dean
Faculty of Engineering & Technology
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 058.

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Academic Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 058

[Handwritten signature]

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

Course Specifications: Full Custom IC Design

Course Title	Full Custom IC Design
Course Code	19VLC501A
Course Type	Core Theory
Department	Electronics and Communication Engineering
Faculty	Engineering and Technology

1. Course Summary

This course deals with design and analysis of CMOS ICs. Students will learn design flow, simulation, and implementation of CMOS based integrated circuits in micro and nanometer technology. This course emphasizes on the design techniques to realize the optimum performance of CMOS ICs in terms of timing, power and area. Reliability issues and the relevant strategies for implementing IC for high yield and manufacturability are discussed.

2. Course Size and Credits:

Number of Credits	04
Credit Structure (Lecture: Tutorial: Practical)	3:0:1
Total Hours of Interaction	75
Number of Weeks in a Semester	15
Department Responsible	Electronics and Communication Engineering
Total Course Marks	100
Pass Criterion	As per the Academic Regulations
Attendance Requirement	As per the Academic Regulations

3. Course Outcomes (COs)

After the successful completion of this course, the student will be able to:

- CO.1. Discuss the concepts of MOS transistors, micro and macro level Integrated Circuits
- CO.2. Analyze, evaluate and recommend appropriate CMOS circuits for development of standard cell libraries and IPs
- CO.3. Model, simulate and analyze the static and dynamic properties of CMOS circuits
- CO.4. Design and optimize CMOS circuits for high performance applications
- CO.5. Use EDA tools to model, design, simulate, analyze and implement the micro and macro level CMOS ICs

4. Course Contents

Unit 1 (MOSFET and Its Characteristics): Introduction to MOS transistor, structure and its types, MOS transistor characteristics, small signal model of MOS transistor, second order effects on MOS behavior, MOS transistor capacitances, model parameters, different level of MOS model equations, types MOS inverter, design of CMOS inverter, DC characteristic analysis, Transient analysis, CMOS inverter static and dynamic power, CMOS inverter load capacitance and interconnection parasitic.

Unit 2 (CMOS Logic Design): Introduction, CMOS logic circuits, complex logic circuits, clocked CMOS

logic, pass transistor logic, CMOS transmission gates, problems of charge sharing, pre-charging techniques,

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Page 30 of 94
Academic Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 054

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

behavior of bistable elements, timing metrics, SR latch and flip-flop circuits, mux-based latches, clocked latch and flip-flop circuit. Case study of combinational and sequential circuits for timing, area and power, Logical effort, transistor sizing, delays in CMOS logic gates, fan-in and fan-out consideration, fast complex gate techniques, computing of logical effort, path and branch effort, multistage delay and best stage effort.

Unit 3 (Memory Design): Introduction, need for memories, classification of memories, Dynamic Random Access Memory (DRAM) and Static Random Access Memory (SRAM), memory architectures, 6T SRAM memory cell architecture, peripheral memory circuitry - sense amplifier, read/write circuitry, bit line pre-charge circuitry, row and column decoders and memory timing, power dissipation, static and dynamic power dissipation, techniques for reduction of power dissipation, low power design through voltage scaling, estimation and optimization of switching activity, reduction of switched capacitance.

Unit 4 (Layout Design): Stick diagram, symbolic diagram, design rules-lambda and micron rules, layout and physical verification, type's full custom layout - data path layout, custom digital layout, cell layout and analog layout, guideline of transistor layout, pMOS and nMOS transistor layout, CMOS transistor layout, sharing diffusion methods, optimization of schematic diagram using dual graph methods and Euler's path, combinational and sequential circuit layout, guard ring protection for digital circuits, analog layout techniques, multi finger, interdigitization, axis of symmetry, common centroid, centroid of array, matched device technique, dummy devices on surrounding, passive component layout - capacitor, resistor and inductor, mixed signal layout issues.

Unit 5 (Standard Cell Design): Classification of STD cell, standard cell design consideration, cell setting, STD cell layout template creation. STD cell Performance for varies process corners, introduction to reliability in CMOS, electro migration, electro migration reduction techniques, cross talk, Effects of cross talk, IR drop, antenna effect, hot electron effect, latch up problem and latch up prevention.

5. Course Map (CO-PO-PSO Map)

	Programme Outcomes (POs)												Programme Specific Outcomes (PSOs)		
	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PO-7	PO-8	PO-9	PO-10	PO-11	PO-12	PSO-1	PSO-2	PSO-3
CO-1	3								1			1	3		1
CO-2	3								1			1	3		1
CO-3	1	3	3	2					1			1	3	2	1
CO-4	1	3	3	2		2	1	2	1	3		1	3	2	3
CO-5					3	1				3		1		3	3

3: Very Strong Contribution, 2: Strong Contribution, 1: Moderate Contribution

6. Course Teaching and Learning Methods

Teaching and Learning Methods	Duration in hours	Total Duration in Hours
Face to Face Lectures		40
Demonstrations		05
1. Demonstration using Videos	05	
2. Demonstration using Physical Models / Systems	00	
3. Demonstration on a Computer	00	

Numeracy Academic Registrar

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



M.S. Ramaiah University of Applied Sciences
Bengaluru - 560 054

Handwritten signature

Page 31 of 94

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

1. Solving Numerical Problems	00	
Practical Work		
1. Course Laboratory	30	30
2. Computer Laboratory	00	
3. Engineering Workshop / Course/Workshop / Kitchen	00	
4. Clinical Laboratory	00	
5. Hospital	00	
6. Model Studio	00	
Others		
1. Case Study Presentation	00	00
2. Guest Lecture	00	
3. Industry / Field Visit	00	
4. Brain Storming Sessions	00	
5. Group Discussions	00	
6. Discussing Possible Innovations	00	
Term Tests, Laboratory Examination/Written Examination, Presentations		10
Total Duration in Hours		85

7. Course Assessment and Reassessment

The details of the components and subcomponents of course assessment are presented in the Programme Specifications document pertaining to the M.Tech. (VLSI and Nanotechnology) Programme. The procedure to determine the final course marks is also presented in the Programme Specifications document.

The evaluation questions are set to measure the attainment of the Cos. In either component (CE or SEE) or subcomponent of CE (SC1, SC2, SC3 or SC4), Cos are assessed as illustrated in the following Table.

Focus of Cos on each Component or Subcomponent of Evaluation					
Subcomponent ▶	Component 1: CE (50% Weightage)				Component 2: SEE (50% Weightage)
	SC1	SC2	SC3	SC4	
Subcomponent Type ▶	Term Test	Assignment	Term Test	Assignment	100 Marks
Maximum Marks ▶	25	25	25	25	
CO-1	X		X		X
CO-2	X		X		X
CO-3		X		X	
CO-4		X		X	
CO-5		X		X	
The details of SC1, SC2, SC3 or SC4 are presented in the Programme Specifications Document.					

The Course Leader assigned to the course, in consultation with the Head of the Department, shall provide the focus of COs in each component of assessment in the above template at the beginning of the semester.

Course reassessment policies are presented in the Academic Regulations document.

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Academic Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore-560054
Page 32 of 94

H.O.

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

8. Achieving COs

The following skills are directly or indirectly imparted to the students in the following teaching and learning methods:

S. No	Curriculum and Capabilities Skills	How imparted during the course
1.	Knowledge	Classroom Lectures
2.	Understanding	Classroom Lectures, Self-study
3.	Critical Skills	Assignment
4.	Analytical Skills	Assignment
5.	Problem Solving Skills	Assignment and Exam
6.	Practical Skills	Assignment
7.	Group Work	Assignment
8.	Self-Learning	Self-learning
9.	Written Communication Skills	Assignment
10.	Verbal Communication Skills	--
11.	Presentation Skills	Assignment
12.	Behavioral Skills	--
13.	Information Management	Assignment
14.	Personal Management	--
15.	Leadership Skills	--

9. Course Resources

a. Essential Reading

1. Behzad Razavi, Design of Analog CMOS Integrated Circuits, McGraw Hill, 2004
2. Sung Kang and Yusuf Leblebici, CMOS Digital integrated circuits, 3rd edition, McGraw Hill, 2004.

b. Recommended Reading

1. J.Rabaey, Digital Integrated Circuits-A design perspective, 2nd edition, Prentice Hall, 2005
2. R. Jacob Baker, CMOS Circuit Design, Layout, and Simulation, 2nd edition, IEEE Press, 2005

c. Website

1. <http://nptel.ac.in/>

10. Course Organization

Course Code	19VLC501A	
Course Title	Full Custom IC Design	
Course Leader's Name	As per Timetable	
Course Leader's Contact Details	Phone:	080-49065555
	E-mail:	hod.ec.et@msruas.ac.in
Course Specifications Approval Date	9-July-2019	
Next Course Specifications Review Date	July-2021	

Dean
Faculty of Engineering & Technology
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 058.

Academic Registrar
M.S. Ramaiah University of Applied Sciences

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Page 33 of 9454

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

Course Specifications: Quantum Mechanics and Nano-electronics

Course Title	Quantum Mechanics and Nano-electronics
Course Code	19VLC502A
Course Type	Core Theory
Department	Electronics and Communication Engineering
Faculty	Engineering and Technology

1. Course Summary

Traditional mechanics serves as basis for electronic engineering. However, it fails to suffice for areas such as, to name one, Nano electronics. With the emergence of quantum engineering and nanotechnology, it is not only desirable but also useful for engineers to become familiar with the basic notions of quantum mechanics. This course focusses on quantum approach of understanding the working of various Nano devices.

2. Course Size and Credits:

Number of Credits	04
Credit Structure (Lecture: Tutorial: Practical)	2:1:1
Total Hours of Interaction	75
Number of Weeks in a Semester	15
Department Responsible	Electronics and Communication Engineering
Total Course Marks	100
Pass Criterion	As per the Academic Regulations
Attendance Requirement	As per the Academic Regulations

3. Course Outcomes (COs)

After the successful completion of this course, the student will be able to:

- CO.1. Perform theoretical studies and calculations with applications on atomic and subatomic phenomena
- CO.2. Gain knowledge on various Nano devices and their working principle
- CO.3. Simulate the basic notion behind quantum mechanics
- CO.4. Evaluate experimental results in terms of quantum mechanics
- CO.5. Apply the knowledge of mathematics, science, and engineering to develop Nano structures and devices

4. Course Contents

Unit 1 (Introduction to Quantum Mechanics): Comparison of classical and quantum systems – origin of quantum mechanics –light as a wave and particle –Electrons as particle and wave-wave packets and uncertainty. Quantum mechanics of electrons – operators for quantum mechanics – Analogies between classical electromagnetics and quantum mechanism.

Unit 2 (Quantum Models): Bohr model and the quantum mechanical model- quantum theory-uncertainty principle -Schrodinger's equation. Probabilistic current density, multiple particle system. Spin and angular momentum. Atomic orbitals –orbital filling – introduction to quantum tunneling – coulomb blockade. Quantum dots – wires- wells. Quantum cellular automata –

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Academic Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 054

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

quantum dot arrays- Digital logic circuit implementations -Quantum dot FPGAs.

Unit 3 (Band Theory): Crystalline materials, Electrons in periodic potential -Kronig-Penney model- band theory of solids –doping –interacting system model- effect of electric field on energy bands – band structures of some semiconductors.

Unit 4 (Evolution of Nano electronics): CMOS transistor scaling theory - short channel effects – Introduction to Nano electronics- challenges, need for Nano devices, circuits and systems. Overview of Nano devices such as CNTFET, FinFET, Nano Wire FET, III/V Compound based devices, Graphene Transistors. Hardware and software tools, Industry trends, research in Nano electronics, Nano products, and future of Nano electronics.

Unit 5 (Fabrication Process of Nano devices): Fabrication methods-Top down methods – lithography types- Bottom up methods - gas-phase methods and liquid phase methods- nanoscale imaging /analysis with microscopes.

5. Course Map (CO-PO-PSO Map)

	Programme Outcomes (POs)												Programme Specific Outcomes (PSOs)		
	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PO-7	PO-8	PO-9	PO-10	PO-11	PO-12	PSO-1	PSO-2	PSO-3
CO-1	3								1			1	3		1
CO-2	3								1			1	3		1
CO-3	1	3	3	2	3				1			1	3	3	1
CO-4	1	3	3	2		2	1	2	1	3		1	3	2	3
CO-5					3	1				3		1		3	3

3: Very Strong Contribution, 2: Strong Contribution, 1: Moderate Contribution

6. Course Teaching and Learning Methods

Teaching and Learning Methods	Duration in hours	Total Duration in Hours
Face to Face Lectures		40
Demonstrations		05
1. Demonstration using Videos	05	
2. Demonstration using Physical Models / Systems	00	
3. Demonstration on a Computer	00	
Numeracy		00
1. Solving Numerical Problems	00	
Practical Work		30
1. Course Laboratory	30	
2. Computer Laboratory	00	
3. Engineering Workshop / Course/Workshop / Kitchen	00	
4. Clinical Laboratory	00	
5. Hospital	00	
6. Model Studio	00	
Others		00
1. Case Study Presentation	00	

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Academic Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 084
Page 35 of 94

Handwritten signature

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

2. Guest Lecture	00	
3. Industry / Field Visit	00	
4. Brain Storming Sessions	00	
5. Group Discussions	00	
6. Discussing Possible Innovations	00	
Term Tests, Laboratory Examination/Written Examination, Presentations	10	
Total Duration in Hours		85

7. Course Assessment and Reassessment

The details of the components and subcomponents of course assessment are presented in the Programme Specifications document pertaining to the M.Tech. (VLSI and Nanotechnology) Programme. The procedure to determine the final course marks is also presented in the Programme Specifications document.

The evaluation questions are set to measure the attainment of the Cos. In either component (CE or SEE) or subcomponent of CE (SC1, SC2, SC3 or SC4), Cos are assessed as illustrated in the following Table.

Focus of Cos on each Component or Subcomponent of Evaluation					
Subcomponent ▶	Component 1: CE (50% Weightage)				Component 2: SEE (50% Weightage)
	SC1	SC2	SC3	SC4	
Subcomponent Type ▶	Term Test	Assignment	Term Test	Assignment	100 Marks
Maximum Marks ▶	25	25	25	25	
CO-1	X		X		X
CO-2	X		X		X
CO-3		X		X	
CO-4		X		X	
CO-5		X		X	
The details of SC1, SC2, SC3 or SC4 are presented in the Programme Specifications Document.					

The Course Leader assigned to the course, in consultation with the Head of the Department, shall provide the focus of COs in each component of assessment in the above template at the beginning of the semester.

Course reassessment policies are presented in the Academic Regulations document.

8. Achieving COs

The following skills are directly or indirectly imparted to the students in the following teaching and learning methods:

S. No	Curriculum and Capabilities Skills	How imparted during the course
1.	Knowledge	Classroom Lectures
2.	Understanding	Classroom Lectures, Self-study
3.	Critical Skills	Assignment
4.	Analytical Skills	Assignment
5.	Problem Solving Skills	Assignment and Exam
6.	Practical Skills	Assignment
7.	Group Work	Assignment



Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

8.	Self-Learning	Self-learning
9.	Written Communication Skills	Assignment
10.	Verbal Communication Skills	--
11.	Presentation Skills	Assignment
12.	Behavioral Skills	--
13.	Information Management	Assignment
14.	Personal Management	--
15.	Leadership Skills	--

9. Course Resources

a. Essential Reading

1. George W. Hanson (2009), Fundamentals of Nano electronics, Pearson Education 1st edition
2. J. Griffiths David (2016) Introduction to Quantum Mechanics, Cambridge India

b. Recommended Reading

1. B. Viswanathan (2009), Nano materials Alpha Science Intl Ltd; 1st edition
2. Robert Pierret (2006), Semiconductor Device Fundamentals, Pearson Education.

c. Website

1. <http://nptel.ac.in/>

10. Course Organization

Course Code	19VLC502A	
Course Title	Quantum Mechanics and Nano electronics	
Course Leader's Name	As per Timetable	
Course Leader's Contact Details	Phone:	080-49065555
	E-mail:	hod.ec.et@msruas.ac.in
Course Specifications Approval Date	09-July-2019	
Next Course Specifications Review Date	July-2021	

Dean
 Faculty of Engineering & Technology
 M.S. Ramaiah University of Applied Sciences
 Bangalore - 560 058.

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Academic Registrar
 M.S. Ramaiah University of Applied Sciences
 Bangalore - 560 054

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

Course Specifications: Semi-Custom IC Design

Course Title	Semi-Custom IC Design
Course Code	19VLC503A
Course Type	Core Theory
Department	Electronics and Communication Engineering
Faculty	Engineering and Technology

1. Course Summary

This course deals with principles of logical synthesis and physical implementation of digital design in semicustom ASIC. Students are guided towards the development of RTL code to derive logical synthesis of a digital design. The concepts of Static Timing Analysis (STA) and Design for Testability (DFT) are emphasized to analyze the performance of synthesized digital design using EDA tool.

2. Course Size and Credits:

Number of Credits	04
Credit Structure (Lecture: Tutorial: Practical)	3:0:1
Total Hours of Interaction	75
Number of Weeks in a Semester	15
Department Responsible	Electronics and Communication Engineering
Total Course Marks	100
Pass Criterion	As per the Academic Regulations
Attendance Requirement	As per the Academic Regulations

3. Course Outcomes (COs)

After the successful completion of this course, the student will be able to:

- CO 1. Discuss concepts of logical and physical designs in semi-custom ASIC design flow
- CO 2. Develop an efficient Register Transfer Logic (RTL) code for a given digital design
- CO 3. Synthesize optimized RTL code for timing, area and power applying suitable constraints
- CO 4. Analyze physical implementation, optimization and verification of synthesized RTL code
- CO 5. Use EDA tools for simulation, synthesis, Static Timing Analysis and Physical implementation of semi-custom ASIC design

4. Course Contents

Unit 1 (Introduction to Semi Custom Design and its attributes): Introduction to semi-custom ASIC design flow, Challenges and opportunities, Need for semi-custom ASICs, Levels of abstraction in VLSI designs, and Semi-custom oriented HDL coding, Different kinds of libraries and their relevance, Operating conditions, Wire-load models, Timing models, Timing arcs, Kinds of standard cells at 130nm, Cell attributes, Footprints, Naming conventions, Terminologies in timing analysis, Various kinds of timing paths, Properties of clock, Clock skew, Timing window and timing violations, Remedies for timing violations, Concept of slack, Critical path, Equations for timing calculations, Solving complex timing problems.



Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

Unit 2 (HDL Modelling of Digital Designs): Introduction to HDL coding, Different levels of Modelling, FSM modelling in Verilog, Logic synthesis with HDL coding, Functions and Tasks, Synthesizable and non-synthesizable constructs, Case study.

Unit 3 (Design Optimization Techniques): Synthesis requirements, Synthesis process, Pareto points, Realization of constraints from specifications, Classes and significance of constraints, Environmental & optimization constraints, Design rule constraints, Timing and power constraints, Point-point exceptions, Chip level constraints, Two level Optimization, Multi-Level optimization, Scheduling and allocation algorithms, Design abstraction levels, Representation domains, Control flow graph, Data flow graph, High level transformations, Low power techniques, Dynamic and leakage power optimization, Multi-VDD, Multi VTH, Retention registers, Top-down and bottom-up synthesis, Characterizing and propagating the constraints, Register pipelining, Multi-Cycle paths.

Unit 4 (Floorplanning in Semi-custom Layout Design): Introduction to floor planning, differentiating between core limited and pad limited design flow, TDF/IO constraint files, defining best aspect ratio, core utilization, chip utilization, flat and hierarchical design flow, partitioning based on timing and interconnects information for hard macros, creating a physical layout, Need for power management, core and IO level power estimation, limitation of core level and IO level power, top to bottom, bottom up approaches, estimating power budget for flattened and hierarchical designs, placement of power mesh (rectangular rings, straps, trunks) and power pads based on IR and EM based criteria.

Unit 5 (Placement and Routing): Introduction to placement, standard cell and macro/DEF placement, timing driven and taming the congestion, detaching scan chains, location constraints, high fanout net synthesis, placement optimization tasks, power optimization, area recovery, Taxonomy of routing, routing algorithms, channel and switch box routing, balanced, and H tree clock routing, routing operations and optimization, density driven routing, post route optimization for timing, performing design finishing processes.

Unit 6 (Clock Tree Synthesis (CTS)): Introduction to CTS, physics of CTS, algorithms for CTS, single and distributed driver scheme, path length and its delay models for skew analysis, balanced clock tree, buffer insertion, constraints and device sizing under process variation in CTS, clock distribution network, low skew and power based global, local and useful skew analysis and optimization methodologies, optimizing yield, interactively cleaning up routing DRC, LVS check and errors, antenna checking and fixing violations, crosstalk prevention, analysis and fixing, design signoff.

5. Course Map (CO-PO-PSO Map)

	Programme Outcomes (POs)												Programme Specific Outcomes (PSOs)		
	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PO-7	PO-8	PO-9	PO-10	PO-11	PO-12	PSO-1	PSO-2	PSO-3
CO-1	3								1			1	3		1
CO-2	3								1			1	3		1
CO-3	1	3	3	2	3				1			1	3	3	1
CO-4	1	3	3	2	3	2	1	2	1	3		1	3	3	3
CO-5					3	1				3		1		3	3

3: Very Strong Contribution, 2: Strong Contribution, 1: Moderate Contribution

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Academic Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 054
Page 39 of 94

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

6. Course Teaching and Learning Methods

Teaching and Learning Methods	Duration in hours	Total Duration in Hours
Face to Face Lectures		40
Demonstrations		05
1. Demonstration using Videos	05	
2. Demonstration using Physical Models / Systems	00	
3. Demonstration on a Computer	00	
Numeracy		00
1. Solving Numerical Problems	00	
Practical Work		30
1. Course Laboratory	30	
2. Computer Laboratory	00	
3. Engineering Workshop / Course/Workshop / Kitchen	00	
4. Clinical Laboratory	00	
5. Hospital	00	
6. Model Studio	00	
Others		00
1. Case Study Presentation	00	
2. Guest Lecture	00	
3. Industry / Field Visit	00	
4. Brain Storming Sessions	00	
5. Group Discussions	00	
6. Discussing Possible Innovations	00	
Term Tests, Laboratory Examination/Written Examination, Presentations		10
Total Duration in Hours		85

7. Course Assessment and Reassessment

The details of the components and subcomponents of course assessment are presented in the Programme Specifications document pertaining to the M.Tech. (VLSI and Nanotechnology) Programme. The procedure to determine the final course marks is also presented in the Programme Specifications document.

The evaluation questions are set to measure the attainment of the Cos. In either component (CE or SEE) or subcomponent of CE (SC1, SC2, SC3 or SC4), Cos are assessed as illustrated in the following Table.

Focus of Cos on each Component or Subcomponent of Evaluation					
Subcomponent ▶	Component 1: CE (50% Weightage)				Component 2: SEE (50% Weightage)
	SC1	SC2	SC3	SC4	
Subcomponent Type ▶	Term Test	Assignment	Term Test	Assignment	100 Marks
Maximum Marks ▶	25	25	25	25	
CO-1	X		X		X
CO-2	X		X		X
CO-3		X		X	

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019

M.S. Ramiah University of Applied Sciences
Bangalore - 560 054

Academic Registrar
M.S. Ramiah University of Applied Sciences
Bangalore - 560 054
Page 40 of 94

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

CO-4		X		X	
CO-5		X		X	
The details of SC1, SC2, SC3 or SC4 are presented in the Programme Specifications Document.					

The Course Leader assigned to the course, in consultation with the Head of the Department, shall provide the focus of COs in each component of assessment in the above template at the beginning of the semester.

Course reassessment policies are presented in the Academic Regulations document.

8. Achieving COs

The following skills are directly or indirectly imparted to the students in the following teaching and learning methods:

S. No	Curriculum and Capabilities Skills	How imparted during the course
1.	Knowledge	Classroom Lectures
2.	Understanding	Classroom Lectures, Self-study
3.	Critical Skills	Assignment
4.	Analytical Skills	Assignment
5.	Problem Solving Skills	Assignment and Exam
6.	Practical Skills	Assignment
7.	Group Work	Assignment
8.	Self-Learning	Self-learning
9.	Written Communication Skills	Assignment
10.	Verbal Communication Skills	--
11.	Presentation Skills	Assignment
12.	Behavioral Skills	--
13.	Information Management	Assignment
14.	Personal Management	--
15.	Leadership Skills	--

9. Course Resources

a. Essential Reading

1. Course Notes
2. Himanshu Bhatnagar (2002). Advanced ASIC Chip Synthesis, Kluwer Academic Publishers.
3. 2. Sung Kyu Lim (2008). Practical Problems in VLSI Physical Design Automation, Springer

b. Recommended Reading

1. Pran Kurup (2003). Logic Synthesis using Synopsys, 2nd edition, Kluwer Academic Publishers.
2. Khosrow Golshan (2007). Physical Design Essentials, Springer

c. Website

1. <http://nptel.ac.in/>

10. Course Organization

Course Code	19VLC503A
Course Title	Semi-Custom IC Design
Course Leader's Name	As per Timetable



Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

Course Leader's Contact Details	Phone:	080-49065555
	E-mail:	hod.ec.et@msruas.ac.in
Course Specifications Approval Date	09-July-2019	
Next Course Specifications Review Date	July-2021	

Dean
Faculty of Engineering & Technology
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 058.

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Academic Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 058
Page 42 of 94

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

Course Specifications: Nano Scale Device Modelling and Simulation

Course Title	Nano Scale Device Modelling and Simulation
Course Code	19VLC504A
Course Type	Core Theory
Department	Electronics and Communication Engineering
Faculty	Engineering and Technology

1. Course Summary

This course deals with nanoscale device physics, modelling and simulations. Application of device physical equations and parameters to model, design, simulate and test the accuracy of the transistor models is covered in this course. The physical meaning of device model parameters and equations; second order effects and high frequency performances are discussed. This course emphasizes on modelling MOSFETs using SPICE and industry standard BSIM models; FinFETs using industry standard BSIM-CMG and BSIM-IMG models. Students are taught to analyze and evaluate the simulation results.

2. Course Size and Credits:

Number of Credits	04
Credit Structure (Lecture: Tutorial: Practical)	2:1:2
Total Hours of Interaction	75
Number of Weeks in a Semester	15
Department Responsible	Electronics and Communication Engineering
Total Course Marks	100
Pass Criterion	As per the Academic Regulations
Attendance Requirement	As per the Academic Regulations

3. Course Outcomes (COs)

After the successful completion of this course, the student will be able to:

- CO 1. Discuss the device physics, theory, models and quantum mechanical effects of MOSFETs and FinFETs
- CO 2. Apply device physics and models to analyze the device characteristics and short channel effects
- CO 3. Model, analyze and evaluate device parameters, characteristics and performance
- CO 4. Model and simulate device characteristics at different technology nodes
- CO 5. Analyze and evaluate device short channel effects using SPICE and BSIM models
- CO 6. Design, simulate, analyze and compare the performance of MOSFET and FinFET based digital circuits using SPICE tools

4. Course Contents

Unit 1 (MOS Physics): MOS capacitor, flat band condition, flat band voltage, surface accumulation, surface depletion, threshold voltage, strong inversion beyond threshold, C – V of MOS capacitor and transistor, oxide charge, poly-Si gate depletion, inversion and accumulation charge layer thicknesses, and quantum mechanical effect.

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Handwritten signature
Academic Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 054

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

Unit 2 (MOSFET Design and Characteristics): Construction of MOSFET, Basic MOSFET operation, drain current, channel length modulation, surface mobility and high mobility FETs, bulk charge effect, basic MOS IV theory, body effect, transconductance, IV characteristics of MOSFETs, velocity saturation, MOS IV theory with velocity saturation, parasitic source-drain resistance, extraction of the series resistance and the effective channel length, MOSFET high frequency performance, MOSFET noises.

Unit 3 (SPICE Modelling of MOSFET): SPICE models for MOS transistor: Level 1, Level 2, Level 3; circuit simulation: the wire, electrical wire models, distributed RC lines in SPICE, transmission line models in SPICE; BSIM series, temperature dependence, process corners, technology scaling, CMOS technology, CMOS Inverter – A circuit example, VTC curve, Inverter speed and power consumption analysis using SPICE.

Unit 4 (FinFET Structure and Characteristics): Limitations of conventional MOSFETs, Multi-gate MOSFET technology, FinFETs, FinFET classification, drain current, characteristics of FinFETs, short channel effects, drain induced barrier lowering, leakage current, FinFET scaling limit, quantum effects in thin body, threshold shift, effective oxide capacitance, FinFET parasitic capacitance, mobility.

Unit 5 (SPICE Modelling of FinFET): FinFET IV- model, C-V model, SPICE models for FinFETs, BSIM CMG FinFET models and BSIM IMG FinFET models, CMOS Inverter using FinFET – A circuit example, VTC curve, Inverter speed and power consumption analysis using SPICE.

5. Course Map (CO-PO-PSO Map)

	Programme Outcomes (POs)												Programme Specific Outcomes (PSOs)		
	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PO-7	PO-8	PO-9	PO-10	PO-11	PO-12	PSO-1	PSO-2	PSO-3
CO-1	3								1			1	3		1
CO-2	3								1			1	3		1
CO-3	1	3	3	2	3				1			1	3	3	1
CO-4	1	3	3	2	3	2	1	2	1	3		1	3	3	3
CO-5	2	1			3	1				3		1	2	3	3
CO-6	1	1	2	2	3	2	1			3		1	2	3	3

3: Very Strong Contribution, 2: Strong Contribution, 1: Moderate Contribution

6. Course Teaching and Learning Methods

Teaching and Learning Methods	Duration in hours	Total Duration in Hours
Face to Face Lectures		40
Demonstrations		05
1. Demonstration using Videos	05	
2. Demonstration using Physical Models / Systems	00	
3. Demonstration on a Computer	00	
Numeracy		00
1. Solving Numerical Problems	00	
Practical Work		30
1. Course Laboratory	30	

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



M.S. Ramaiah University of Applied Sciences
Academic Registrar
Bangalore - 560 084
Page 44 of 94

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

2. Computer Laboratory	00	
3. Engineering Workshop / Course/Workshop / Kitchen	00	
4. Clinical Laboratory	00	
5. Hospital	00	
6. Model Studio	00	
Others		
1. Case Study Presentation	00	
2. Guest Lecture	00	
3. Industry / Field Visit	00	
4. Brain Storming Sessions	00	
5. Group Discussions	00	
6. Discussing Possible Innovations	00	
Term Tests, Laboratory Examination/Written Examination, Presentations		10
Total Duration in Hours		85

7. Course Assessment and Reassessment

The details of the components and subcomponents of course assessment are presented in the Programme Specifications document pertaining to the M.Tech. (VLSI and Nanotechnology) Programme. The procedure to determine the final course marks is also presented in the Programme Specifications document.

The evaluation questions are set to measure the attainment of the Cos. In either component (CE or SEE) or subcomponent of CE (SC1, SC2, SC3 or SC4), Cos are assessed as illustrated in the following Table.

Focus of Cos on each Component or Subcomponent of Evaluation					
Subcomponent ▶	Component 1: CE (50% Weightage)				Component 2: SEE (50% Weightage)
	SC1	SC2	SC3	SC4	
Subcomponent Type ▶	Term Test	Assignment	Term Test	Assignment	100 Marks
Maximum Marks ▶	25	25	25	25	
CO-1	X		X		X
CO-2	X		X		X
CO-3		X	X	X	X
CO-4		X		X	
CO-5		X		X	
CO-6		X		X	

The details of SC1, SC2, SC3 or SC4 are presented in the Programme Specifications Document.

The Course Leader assigned to the course, in consultation with the Head of the Department, shall provide the focus of COs in each component of assessment in the above template at the beginning of the semester.

Course reassessment policies are presented in the Academic Regulations document.

8. Achieving COs

The following skills are directly or indirectly imparted to the students in the following



Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

teaching and learning methods:

S. No	Curriculum and Capabilities Skills	How imparted during the course
1.	Knowledge	Classroom Lectures
2.	Understanding	Classroom Lectures, Self-study
3.	Critical Skills	Assignment
4.	Analytical Skills	Assignment
5.	Problem Solving Skills	Assignment and Exam
6.	Practical Skills	Assignment
7.	Group Work	Assignment
8.	Self-Learning	Self-learning
9.	Written Communication Skills	Assignment
10.	Verbal Communication Skills	--
11.	Presentation Skills	Assignment
12.	Behavioral Skills	--
13.	Information Management	Assignment
14.	Personal Management	--
15.	Leadership Skills	--

9. Course Resources

a. Essential Reading

1. Course Notes
2. Cheng Y. and Hu, C., (2002) Noise Model. MOSFET Modeling & BSIM3 User's Guide, pp.219-241
3. Colinge J.P. ed., (2008) FinFETs and other multi-gate transistors (Vol. 73). New York: Springer

b. Recommended Reading

1. Behzad Razavi (2002) Design of Analog CMOS Integrated Circuits, McGraw Hill
2. Hu C., (2010) Modern semiconductor devices for integrated circuits (Vol. 2). Upper Saddle River, NJ: Prentice Hall

c. Website

1. <http://nptel.ac.in/>

10. Course Organization

Course Code	19VLC504A	
Course Title	Nano Scale Device Modelling and Simulation	
Course Leader's Name	As per Timetable	
Course Leader's Contact Details	Phone:	080-49065555
	E-mail:	hod.ec.et@msruas.ac.in
Course Specifications Approval Date	09-July-2019	
Next Course Specifications Review Date	July-2021	

Dean
Faculty of Engineering & Technology
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 058.

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Academic Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 054

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

Course Specifications: FPGA System Design and Implementation

Course Title	FPGA System Design and Implementation
Course Code	19VLC511A
Course Type	Core Theory
Department	Electronics and Communication Engineering
Faculty	Engineering and Technology

1. Course Summary

This course deals with the implementation of a digital design on FPGA, its re-configurable hardware features and principles of RTL development. This course deals with developing HDL codes for a given digital design. Design implementation optimization and debugging of the digital design on FPGA are also emphasized using EDA tools.

2. Course Size and Credits:

Number of Credits	05
Credit Structure (Lecture: Tutorial: Practical)	4:0:2
Total Hours of Interaction	90
Number of Weeks in a Semester	15
Department Responsible	Electronics and Communication Engineering
Total Course Marks	100
Pass Criterion	As per the Academic Regulations
Attendance Requirement	As per the Academic Regulations

3. Course Outcomes (COs)

After the successful completion of this course, the student will be able to:

- CO 1. Discuss the methodologies involved in design, verification and implementation of digital designs on reconfigurable hardware platform (FPGA)
- CO 2. Discuss and analyze different FPGA Architectures and significance of components of architectures.
- CO 3. Develop optimized design for area, timing and power by applying suitable constraints
- CO 4. Develop efficient synthesizable HDL code for hardware realization of a given digital design
- CO 5. Use EDA tools to develop, verify and implement digital design on reconfigurable

4. Course Contents

Unit 1 (Introduction of FPGA): Introduction to VLSI systems and reconfigurable systems, Need for reconfigurable systems, Design flow of VLSI, Two competing implementation - ASIC & FPGA, Major FPGA vendors, The reconfigurable marketplace, PLD market share, Std Cell ASIC Development Cost Trend, Today's typical design, Importance of reconfigurable systems in VLSI design, Application for reconfigurable systems, Future of reconfigurable systems, Introduction to FPGAs, Need of FPGAs in DSP Applications, DSP Processors vs. FPGAs, Product Roadmap, Review of PLA, PAL, Introduction to PLDs, Concept of CLB, Interconnect structure, ROM, PROM, Introduction to FPGA, FPGA vendors, FPGA structures.

Unit 2 (Advanced Digital Designs): Introduction to VLSI Designs and advanced digital design

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



M.S. Ramaiah University of Applied Sciences
Academic Registrar
Page 47 of 94
Contact: 080 054

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

(Multipliers, Adders and FSM's), Review of PLA, PAL, PLDs. FPGAs Vs DSP Processors, Multipliers, Booth encoding scheme, Wallace tree, FIFO modelling, Finite state machines, FSM modelling in Verilog, Functions and Tasks, UDPs, Case study – FIFO

Unit 3 (FPGA Architectures): Introduction to FPGA Architecture, Different FPGA Architectures, Components of FPGA Architectures - Programming Technology, Antifuse, Static RAM, EPROM, EEPROM technology, Logic elements and Lookup Tables, Dedicated multipliers, Block and Distributed RAM, Shift registers, Digital Clock Managers and Macros.

Unit 4 (FPGA Implementation): Synthesis, Translate, Map, Floorplan, Place and Route, UCF, constraints, FPGA programming, Reading and analysing reports-post synthesis, Case study

Unit 5 (Constraints and Debugging): Timing analysis, slack calculation, Period constraints, Offset IN, Offset OUT, FPGA Debugging and Advanced FPGA: Introduction and usage of IP, Introduction to FPGA, Debugging, Debugging using chip scope and Logic analyzers, High Speed SERDES

5. Course Map (CO-PO-PSO Map)

	Programme Outcomes (POs)												Programme Specific Outcomes (PSOs)		
	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PO-7	PO-8	PO-9	PO-10	PO-11	PO-12	PSO-1	PSO-2	PSO-3
CO-1	3								1			1	3		1
CO-2	3								1			1	3		1
CO-3	1	3	3	2					1			1	3	2	1
CO-4	1	3	3	2		2	1	2	1	3		1	3	2	3
CO-5					3	1				3		1		3	3

3: Very Strong Contribution, 2: Strong Contribution, 1: Moderate Contribution

6. Course Teaching and Learning Methods

Teaching and Learning Methods	Duration in hours	Total Duration in Hours
Face to Face Lectures		45
Demonstrations		15
1. Demonstration using Videos	10	
2. Demonstration using Physical Models / Systems	00	
3. Demonstration on a Computer	05	
Numeracy		00
1. Solving Numerical Problems	00	
Practical Work		30
1. Course Laboratory	30	
2. Computer Laboratory	00	
3. Engineering Workshop / Course/Workshop / Kitchen	00	
4. Clinical Laboratory	00	
5. Hospital	00	
6. Model Studio	00	
Others		00

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Academic Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 084
Page 48 of 94

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

1. Case Study Presentation	05	
2. Guest Lecture	00	
3. Industry / Field Visit	00	
4. Brain Storming Sessions	00	
5. Group Discussions	00	
6. Discussing Possible Innovations	00	
Term Tests, Laboratory Examination/Written Examination, Presentations	10	
Total Duration in Hours	85	

7. Course Assessment and Reassessment

The details of the components and subcomponents of course assessment are presented in the Programme Specifications document pertaining to the M.Tech. (VLSI and Nanotechnology) Programme. The procedure to determine the final course marks is also presented in the Programme Specifications document.

The evaluation questions are set to measure the attainment of the COs. In either component (CE or SEE) or subcomponent of CE (SC1, SC2, SC3 or SC4), Cos are assessed as illustrated in the following Table.

Focus of Cos on each Component or Subcomponent of Evaluation					
Subcomponent ▶	Component 1: CE (50% Weightage)				Component 2: SEE (50% Weightage)
	SC1	SC2	SC3	SC4	
Subcomponent Type ▶	Term Test	Assignment	Term Test	Assignment	100 Marks
Maximum Marks ▶	25	25	25	25	
CO-1	X				X
CO-2	X		X		X
CO-3		X	X	X	X
CO-4		X		X	
CO-5		X		X	

The details of SC1, SC2, SC3 or SC4 are presented in the Programme Specifications Document.

The Course Leader assigned to the course, in consultation with the Head of the Department, shall provide the focus of COs in each component of assessment in the above template at the beginning of the semester.

Course reassessment policies are presented in the Academic Regulations document.

8. Achieving COs

The following skills are directly or indirectly imparted to the students in the following teaching and learning methods:

S. No	Curriculum and Capabilities Skills	How imparted during the course
1.	Knowledge	Classroom Lectures
2.	Understanding	Classroom Lectures, Self-study
3.	Critical Skills	Assignment
4.	Analytical Skills	Assignment
5.	Problem Solving Skills	Assignment and Exam
6.	Practical Skills	Assignment
7.	Group Work	Assignment



Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

8.	Self-Learning	Self-learning
9.	Written Communication Skills	Assignment
10.	Verbal Communication Skills	--
11.	Presentation Skills	Assignment
12.	Behavioral Skills	--
13.	Information Management	Assignment
14.	Personal Management	--
15.	Leadership Skills	--

9. Course Resources

a. Essential Reading

1. Course Notes
2. Michael D. Ciletti (2010). Advanced Digital Design with the Verilog HDL, 4th edition, Pearson Education.
3. Samir Palnitkar (2012). Verilog HDL, 5th edition, Prentice Hall.

b. Recommended Reading

1. Clive Max Field (2004). The design. Warriors Guide to FPGA, Elsevier.
2. Stuart Sutherland (2002). Verilog 2001, Kluwer Academic Publishers.

c. Website

1. <http://nptel.ac.in/>

10. Course Organization

Course Code	19VLC511A	
Course Title	FPGA System Design and Implementation	
Course Leader's Name	As per Timetable	
Course Leader's Contact Details	Phone:	080-49065555
	E-mail:	hod.ec.et@msruas.ac.in
Course Specifications Approval Date	09-July-2019	
Next Course Specifications Review Date	July-2021	



Dean
Faculty of Engineering & Technology
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 058.

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019

Academic Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 054

Page 50 of 94

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

Course Specifications: Nano Materials and Devices

Course Title	Nano Materials and Devices
Course Code	19VLC512A
Course Type	Core Theory
Department	Electronics and Communication Engineering
Faculty	Engineering and Technology

1. Course Summary

This course provides the basic concepts involved in Nanotechnology i.e. from materials to device fabrication and characterization. The course emphasis on different nanostructures and their properties. New Nano scale devices and circuit designs are introduced to the students. Nano sensors and their applications are also covered in this course.

2. Course Size and Credits:

Number of Credits	05
Credit Structure (Lecture: Tutorial: Practical)	4:0:2
Total Hours of Interaction	90
Number of Weeks in a Semester	15
Department Responsible	Electronics and Communication Engineering
Total Course Marks	100
Pass Criterion	As per the Academic Regulations
Attendance Requirement	As per the Academic Regulations

3. Course Outcomes (COs)

After the successful completion of this course, the student will be able to:

- CO 1. Discuss the working principles of various Nano devices
- CO 2. Design electronic circuits using Nano devices
- CO 3. Analyze the Nano circuits design and optimize it for high performance
- CO 4. Acquire knowledge on the fabrication of nanostructures from materials
- CO 5. Apply the knowledge of device physics in nanoscale engineering

4. Course Contents

Unit 1 (Nanomaterial and its types): Properties of nanomaterials -mechanical, electrical, optical and magnetic properties. Types of Nano materials – carbon, metal and group III-V semiconductor compound based Nano materials- Zero, One, Two and Three dimensional nanostructured materials. Quantum dots, Graphene sheets- properties- fabrication of graphene sheets- bandgap opening techniques. Graphene Nano ribbon –Types -Carbon Nano tubes (CNT) - classification/structure, properties of CNTs, fabrication/growth methods of CNTs. Types of CNTs- single and double wall nano- tube. Electrical and mechanical properties of CNTs. Metallic and semiconducting CNTs. Effect of twisting and bending on band gap- Applications of CNTs.

Unit 2 (Graphene and CNT Transistor): Graphene Transistors formation process, Modeling and simulation of Graphene transistor, Analog and digital circuit's implementation. FETs



Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

using CNT- fabrication-single and multichannel FET, single and multiwall FETs. Circuit implementations - Application of CNTFET in VLSI.

Unit 3 (Tunneling Diode and Single Electron Transistor): Tunneling Diode, Resonant Tunneling Diode (RTD), Three terminal resonant tunneling devices, Technology of RTD, digital circuit based on RTDs –, basic Logic Circuits. Memory applications. Single Electron Transistor (SET) - Principles of SET, circuit design using SET.

Unit 4 (Logic Design using FinFET): Short gate effects of MOS, Independent gate FinFETs, logic design using SG/IG mode FinFETs, Threshold voltage control through multiple supply voltage for power efficient FinFET, interconnects, Principle of TCMS, Logic design using TCMS, Latch design using SG/IG mode FinFETs, FinFET Domino logic, Design and analysis of FinFET SRAM.

Unit 5 (Nanosensors): Advantages and applications- CNFFET as sensor- artificial nose. Nano wire as sensor- PH sensor, protein, DNA sensor and optical Nano sensor

5. Course Map (CO-PO-PSO Map)

	Programme Outcomes (POs)												Programme Specific Outcomes (PSOs)		
	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PO-7	PO-8	PO-9	PO-10	PO-11	PO-12	PSO-1	PSO-2	PSO-3
CO-1	3								1			1	3		1
CO-2	3								1			1	3		1
CO-3	1	3	3	2					1			1	3	2	1
CO-4	1	3	3	2		2	1	2	1	3		1	3	2	3
CO-5					3	1				3		1		3	3

3: Very Strong Contribution, 2: Strong Contribution, 1: Moderate Contribution

6. Course Teaching and Learning Methods

Teaching and Learning Methods	Duration in hours	Total Duration in Hours
Face to Face Lectures		45
Demonstrations		15
1. Demonstration using Videos	10	
2. Demonstration using Physical Models / Systems	00	
3. Demonstration on a Computer	05	
Numeracy		00
1. Solving Numerical Problems	00	
Practical Work		30
1. Course Laboratory	30	
2. Computer Laboratory	00	
3. Engineering Workshop / Course/Workshop / Kitchen	00	
4. Clinical Laboratory	00	
5. Hospital	00	
6. Model Studio	00	
Others		00

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Academic Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 054

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

1. Case Study Presentation	05	
2. Guest Lecture	00	
3. Industry / Field Visit	00	
4. Brain Storming Sessions	00	
5. Group Discussions	00	
6. Discussing Possible Innovations	00	
Term Tests, Laboratory Examination/Written Examination, Presentations	10	
Total Duration in Hours	100	

7. Course Assessment and Reassessment

The details of the components and subcomponents of course assessment are presented in the Programme Specifications document pertaining to the M.Tech. (VLSI and Nanotechnology) Programme. The procedure to determine the final course marks is also presented in the Programme Specifications document.

The evaluation questions are set to measure the attainment of the COs. In either component (CE or SEE) or subcomponent of CE (SC1, SC2, SC3 or SC4), Cos are assessed as illustrated in the following Table.

Focus of Cos on each Component or Subcomponent of Evaluation					
Subcomponent ▶	Component 1: CE (50% Weightage)				Component 2: SEE (50% Weightage)
	SC1	SC2	SC3	SC4	
Subcomponent Type ▶	Term Test	Assignment	Term Test	Assignment	100 Marks
Maximum Marks ▶	25	25	25	25	
CO-1	X				X
CO-2	X		X		X
CO-3		X	X	X	X
CO-4		X		X	
CO-5		X		X	

The details of SC1, SC2, SC3 or SC4 are presented in the Programme Specifications Document.

The Course Leader assigned to the course, in consultation with the Head of the Department, shall provide the focus of COs in each component of assessment in the above template at the beginning of the semester.

Course reassessment policies are presented in the Academic Regulations document.

8. Achieving COs

The following skills are directly or indirectly imparted to the students in the following teaching and learning methods:

S. No	Curriculum and Capabilities Skills	How imparted during the course
1.	Knowledge	Classroom Lectures
2.	Understanding	Classroom Lectures, Self-study
3.	Critical Skills	Assignment
4.	Analytical Skills	Assignment
5.	Problem Solving Skills	Assignment and Exam
6.	Practical Skills	Assignment
7.	Group Work	Assignment

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Academic Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 054

Handwritten signature

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

8.	Self-Learning	Self-learning
9.	Written Communication Skills	Assignment
10.	Verbal Communication Skills	--
11.	Presentation Skills	Assignment
12.	Behavioral Skills	--
13.	Information Management	Assignment
14.	Personal Management	--
15.	Leadership Skills	--

9. Course Resources

a. Essential Reading

1. Course Notes
2. Niraj K. Jha, Deming Chen (2008), Nano electronic Circuit Design, Springer. Gregory Timp. Nanotechnology, AIP Press.
3. B. Viswanathan (2009), Nano materials Alpha Science Intl Ltd; 1st edition

b. Recommended Reading

1. Goser Karl and Peter Glosekotter. (2004) Nanoelectronics and Nanosystems: From Transistors to Molecular and Quantum Devices, Springer
2. S. Dutta. (2005) Quantum Transport: Atom to Transistor, Cambridge University Press.

c. Website

1. <http://nptel.ac.in/>

10. Course Organization

Course Code	19VLC512A	
Course Title	Nano Materials and Devices	
Course Leader's Name	As per Timetable	
Course Leader's Contact Details	Phone:	080-49065555
	E-mail:	hod.ec.et@msruas.ac.in
Course Specifications Approval Date	09-July-2019	
Next Course Specifications Review Date	July-2021	

Dean
Faculty of Engineering & Technology
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 058.

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Academic Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 054

Handwritten signature

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

Course Specifications: VLSI Verification and Testing

Course Title	VLSI Verification and Testing
Course Code	19VLE512A
Course Type	Professional Core Elective
Department	Electronics and Communication Engineering
Faculty	Engineering and Technology

1. Course Summary

This course focuses on the importance of design verification and testing in VLSI design. The students will learn the methodologies for design verification and analysis of performance of design after inclusion of verification courses. The course also deals with issues associated with DFT techniques, fault modelling and BIST Circuits.

2. Course Size and Credits:

Number of Credits	04
Credit Structure (Lecture: Tutorial: Practical)	4:0:0
Total Hours of Interaction	60
Number of Weeks in a Semester	15
Department Responsible	Electronics and Communication Engineering
Total Course Marks	100
Pass Criterion	As per the Academic Regulations
Attendance Requirement	As per the Academic Regulations

3. Course Outcomes (COs)

After the successful completion of this course, the student will be able to:

- CO 1. Discuss different functional verification methodologies and different aspects of hardware verification language
- CO 2. Discuss need of IC testing, fault modelling and simulations and different techniques for testing
- CO 3. Develop and analyze functional verification environment using hardware verification languages and different components of functional verification
- CO 4. Analyze different testing approaches and DFT techniques at various design hierarchies
- CO 5. Perform verification of an IC and apply designs for testing and optimize the design using standard CAD tools

4. Course Contents

Unit 1 (Introduction to System Verilog): System Verilog enhancements to Verilog 2001, Generations of System Verilog standard and enhancements for hardware design, System Verilog dot name and dot star enhancements, Case study on instantiation example for complex ALU, data types and operators, static and automatic variables, structure declarations, types of arrays, procedural blocks.

Unit 2 (Verification and its components): Need for verification, Verification process, challenges in verification, cost involved, time involved, verification methodologies and techniques, mission and goals of verification, verification plans, verification flow and guidelines, Industry standard

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Academic Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 054

[Handwritten signature]

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

verification, Assertions concepts, Types of assertion, coverage types, functional coverage strategies, cover group, coverage options, analysing coverage data, measuring coverage statistics during simulation.

Unit 3 (Verification Methodologies): Introduction to Verification Methodologies, Verification strategy using UVM, constraint details, common randomization problems, random control, random generators, random device configuration, agent, scoreboard, checker, driver, monitor and other functional layers, building a complete verification environment, bootstrapping the verification process, high-level modelling concepts, coverage directed generation, verification coverage, program and clocking blocks, active and reactive regions, inter-process communication, advanced interfaces.

Unit 4 (VLSI Testing): Need for testing, Importance of testing, Role of testing, Trends in testing, Test cost estimates, DFT cycle, Basic definitions like defect, fault and error, Testing at different levels, Difficulties and challenges of VLSI testing, VLSI chip yield, Fault coverage and defect level, Discussion of reliability issues, Basics of DFM, Importance of fault modelling, Single stuck at fault, Multiple stuck at faults, Bridging faults, Pattern sensitive faults, Transistor faults, Cross point fault, Delay fault, Test and test set, Fault collapsing, Fault simulation concepts, Fault simulation approaches.

Unit 5 (Design for Test(DFT)): DFT Introduction, Controllability, Observability, Need for DFT, DFT techniques, Adhoc DFT, Structured DFT, Scan based design, Scan flip-flop, Different scan types, Scan design rules, RTL for DFT, Test mode vs. Scan mode, DFT DRC rules, Scan clock skew, Multiple test insertion, Adding scan structure, Scan overheads, BIST Architecture, Pseudo-Random generators, Signature analysis, Linear Feedback Shift Registers (LFSR) as pattern generators, LFSR as signature analyzers, Built in Logic Block Observers (BILBO).

5. Course Map (CO-PO-PSO Map)

	Programme Outcomes (POs)												Programme Specific Outcomes (PSOs)		
	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PO-7	PO-8	PO-9	PO-10	PO-11	PO-12	PSO-1	PSO-2	PSO-3
CO-1	3								1			1	3		1
CO-2	3								1			1	3		1
CO-3	1	3	3	2					1			1	3	2	1
CO-4	1	3	3	2		2	1	2	1	3		1	3	2	3
CO-5					3	1				3		1		3	3

3: Very Strong Contribution, 2: Strong Contribution, 1: Moderate Contribution

6. Course Teaching and Learning Methods

Teaching and Learning Methods	Duration in hours	Total Duration in Hours
Face to Face Lectures		40
Demonstrations		05
1. Demonstration using Videos	05	
2. Demonstration using Physical Models / Systems	00	
3. Demonstration on a Computer	00	
Numeracy		00
1. Solving Numerical Problems	00	

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Academic Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 054

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

Practical Work		00
1. Course Laboratory	00	
2. Computer Laboratory	00	
3. Engineering Workshop / Course/Workshop / Kitchen	00	
4. Clinical Laboratory	00	
5. Hospital	00	
6. Model Studio	00	
Others		15
1. Case Study Presentation	15	
2. Guest Lecture	00	
3. Industry / Field Visit	00	
4. Brain Storming Sessions	00	
5. Group Discussions	00	
6. Discussing Possible Innovations	00	
Term Tests, Laboratory Examination/Written Examination, Presentations		10
Total Duration in Hours		70

7. Course Assessment and Reassessment

The details of the components and subcomponents of course assessment are presented in the Programme Specifications document pertaining to the M.Tech. (VLSI and Nanotechnology) Programme. The procedure to determine the final course marks is also presented in the Programme Specifications document.

The evaluation questions are set to measure the attainment of the COs. In either component (CE or SEE) or subcomponent of CE (SC1, SC2, SC3 or SC4), Cos are assessed as illustrated in the following Table.

Focus of Cos on each Component or Subcomponent of Evaluation					
Subcomponent ▶	Component 1: CE (50% Weightage)				Component 2: SEE (50% Weightage)
	SC1	SC2	SC3	SC4	
Subcomponent Type ▶	Term Test	Assignment	Term Test	Assignment	100 Marks
Maximum Marks ▶	25	25	25	25	
CO-1	X				X
CO-2	X		X		X
CO-3		X	X	X	X
CO-4		X		X	
CO-5		X		X	

The details of SC1, SC2, SC3 or SC4 are presented in the Programme Specifications Document.

The Course Leader assigned to the course, in consultation with the Head of the Department, shall provide the focus of COs in each component of assessment in the above template at the beginning of the semester.

Course reassessment policies are presented in the Academic Regulations document.

8. Achieving COs

The following skills are directly or indirectly imparted to the students in the following

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Academic Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 054

H/O

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

teaching and learning methods:

S. No	Curriculum and Capabilities Skills	How imparted during the course
1.	Knowledge	Classroom Lectures
2.	Understanding	Classroom Lectures, Self-study
3.	Critical Skills	Assignment
4.	Analytical Skills	Assignment
5.	Problem Solving Skills	Assignment and Exam
6.	Practical Skills	Assignment
7.	Group Work	Assignment
8.	Self-Learning	Self-learning
9.	Written Communication Skills	Assignment
10.	Verbal Communication Skills	--
11.	Presentation Skills	Assignment
12.	Behavioral Skills	--
13.	Information Management	Assignment
14.	Personal Management	--
15.	Leadership Skills	--

9. Course Resources

a. Essential Reading

1. Course Notes
2. Chris Spear, System Verilog for Verification, 2nd edition, Springer, 2004
3. Andrew Piziali, Functional Verification Coverage Measurement and Analysis, Kluwer Academic Publications, 2004

b. Recommended Reading

1. Vishwani D. Agrawal and Michael L. Bushnell, Essentials of Electronic Testing, Kluwer Academic Publishers, 2004
2. Laung Terng Wang, Cheng Wen Wu and Xiaogeng Wen, VLSI Test Principles & Architectures, Morgan Kaufman Publishers, 2006

c. Website

1. <http://nptel.ac.in/>

10. Course Organization

Course Code	19VLE512A	
Course Title	VLSI Verification and Testing	
Course Leader's Name	As per Timetable	
Course Leader's Contact Details	Phone:	080-49065555
	E-mail:	hod.ec.et@msruas.ac.in
Course Specifications Approval Date	09-July-2019	
Next Course Specifications Review Date	July-2021	

Dean
 Faculty of Engineering & Technology
 M.S. Ramaiah University of Applied Sciences
 Bangalore - 560 058.

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Page 58 of 94
 Academic Registrar
 M.S. Ramaiah University of Applied Sciences
 Bangalore - 560 054

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

Course Specifications: Analog and Mixed Signal Circuit Design

Course Title	Analog and Mixed Signal Circuit Design
Course Code	19VLE513A
Course Type	Professional Core Elective
Department	Electronics and Communication Engineering
Faculty	Engineering and Technology

1. Course Summary

This course focuses on the importance of CMOS and mixed signal VLSI design in the field of electronics and telecommunication. The students will learn the methodologies for design and analysis of basic CMOS analog and mixed signal circuits like current mirrors, single stage amplifiers, operational amplifiers, data converters, comparators and phase locked loops. The course also deals with issues associated with high performance mixed signal VLSI Circuits.

2. Course Size and Credits:

Number of Credits	04
Credit Structure (Lecture: Tutorial: Practical)	4:0:0
Total Hours of Interaction	60
Number of Weeks in a Semester	15
Department Responsible	Electronics and Communication Engineering
Total Course Marks	100
Pass Criterion	As per the Academic Regulations
Attendance Requirement	As per the Academic Regulations

3. Course Outcomes (COs)

After the successful completion of this course, the student will be able to:

- CO 1. Gain knowledge on the working and design principles of analog and mixed signal circuits
- CO 2. Design and analyze CMOS mixed signal circuits for a given specification
- CO 3. Acquire knowledge on design different architectures in mixed signal mode.
- CO 4. Analyze and optimize the circuits for achieving high performance
- CO 5. Use EDA tools to model, design, simulate, analyze and implement analog, digital, and mixed signal circuits

4. Course Contents

Unit 1 (Amplifier using MOSFET): Biasing of MOS transistor for analog applications, current-voltage characteristics, Design of analog circuits such as current mirror, single stage amplifier, differential amplifier and Op-Amp. Analysis and optimization of static, transient and frequency performance of analog circuits, Importance and properties of feedback circuit, Different types of feedback topology, Stability and frequency compensation of two stage Op-Amp.

Unit 2 (Switched Capacitor Circuits): Switched capacitor circuits and its general consideration, Analysis of various switched capacitor amplifier circuits and its applications, Design and analysis switched capacitor filter circuits, Design and Analysis of various switched capacitor integrator circuits. MOSFET as switch- Noise analysis.

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Academic Registrar
M.S. Ramiah University of Applied Sciences
Page 59 of 94
Bangalore - 560 054

H/O

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

Unit 3 (Comparators): Static and dynamic characteristic of comparator, Analysis two stage open loop comparators and its performance, Design and simulation analysis of two stage open loop comparator design, improving performance of open loop comparator, Discrete time comparators – switched capacitor comparator, regenerate comparator, High-speed comparators.

Unit 4 (Analog to Digital Converters(ADC) and Digital to Analog Converters(DAC)): Static and transient design specifications of ADC - DNL, INL, offset error, gain error, latency, dynamic range, SNR, SFDR and ENOB, ADC architectures – Flash, Two step flash, pipeline, Integrated, successive approximation and oversampling ADC, Mismatches and accuracy issues. Analog versus discrete time signal and sample and hold characteristic, Static and transient design specifications of DAC – DNL, INL, offset error, gain error, latency, dynamic range, SNR, SFDR and ENOB, DAC architectures – resistor string, R-2R, current mode, voltage mode, current steering, charge scaling, cyclic and pipeline ADC, Mismatches error related resistor and current steering DAC.

Unit 5 (Phase Locked Loop (PLL)): Types of PLL and its operation, Design specification of PLL, Design of PLL subsystems – Phase Frequency Detector, charge pump, Voltage Controlled Oscillators and loop filter, Non ideal effects in PLL, PLL applications - Frequency multiplication and synthesis . ALL digital PLLs.

5. Course Map (CO-PO-PSO Map)

	Programme Outcomes (POs)												Programme Specific Outcomes (PSOs)		
	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PO-7	PO-8	PO-9	PO-10	PO-11	PO-12	PSO-1	PSO-2	PSO-3
CO-1	3											1	3		1
CO-2	3											1	3		1
CO-3	3	3	3	1								1	3		1
CO-4	3	3	3	1		2	1	2	1			1	3	2	2
CO-5	3	3	3	1		2	1	2	1	3		1	3	2	3

3: Very Strong Contribution, 2: Strong Contribution, 1: Moderate Contribution

6. Course Teaching and Learning Methods

Teaching and Learning Methods	Duration in hours	Total Duration in Hours
Face to Face Lectures		40
Demonstrations		05
1. Demonstration using Videos	05	
2. Demonstration using Physical Models / Systems	00	
3. Demonstration on a Computer	00	
Numeracy		15
1. Solving Numerical Problems	15	
Practical Work		00
1. Course Laboratory	00	
2. Computer Laboratory	00	
3. Engineering Workshop / Course/Workshop / Kitchen	00	
4. Clinical Laboratory	00	
5. Hospital	00	

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



M.S. Ramaiah University of Applied Sciences
Academic Registrar
Page 60 of 94
Bangalore - 560 054

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

6. Model Studio	00	
Others		
1. Case Study Presentation	00	00
2. Guest Lecture	00	
3. Industry / Field Visit	00	
4. Brain Storming Sessions	00	
5. Group Discussions	00	
6. Discussing Possible Innovations	00	
Term Tests, Laboratory Examination/Written Examination, Presentations		10
Total Duration in Hours		70

7. Course Assessment and Reassessment

The details of the components and subcomponents of course assessment are presented in the Programme Specifications document pertaining to the M.Tech. (VLSI and Nanotechnology) Programme. The procedure to determine the final course marks is also presented in the Programme Specifications document.

The evaluation questions are set to measure the attainment of the COs. In either component (CE or SEE) or subcomponent of CE (SC1, SC2, SC3 or SC4), Cos are assessed as illustrated in the following Table.

Focus of Cos on each Component or Subcomponent of Evaluation					
Subcomponent ▶	Component 1: CE (50% Weightage)				Component 2: SEE (50% Weightage)
	SC1	SC2	SC3	SC4	
Subcomponent Type ▶	Term Test	Assignment	Term Test	Assignment	100 Marks
Maximum Marks ▶	25	25	25	25	
CO-1	X				X
CO-2	X		X		X
CO-3	X	X	X	X	X
CO-4		X	X	X	
CO-5		X		X	

The details of SC1, SC2, SC3 or SC4 are presented in the Programme Specifications Document.

The Course Leader assigned to the course, in consultation with the Head of the Department, shall provide the focus of COs in each component of assessment in the above template at the beginning of the semester.

Course reassessment policies are presented in the Academic Regulations document.

8. Achieving COs

The following skills are directly or indirectly imparted to the students in the following teaching and learning methods:

S. No	Curriculum and Capabilities Skills	How imparted during the course
1.	Knowledge	Classroom Lectures
2.	Understanding	Classroom Lectures, Self-study
3.	Critical Skills	Assignment
4.	Analytical Skills	Assignment
5.	Problem Solving Skills	Assignment and Exam

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Academic Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 054
Page 61 of 94

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

6.	Practical Skills	Assignment
7.	Group Work	Assignment
8.	Self-Learning	Self-learning
9.	Written Communication Skills	Assignment
10.	Verbal Communication Skills	--
11.	Presentation Skills	Assignment
12.	Behavioral Skills	--
13.	Information Management	Assignment
14.	Personal Management	--
15.	Leadership Skills	--

9. Course Resources

a. Essential Reading

1. Course Notes
2. Behzad Razavi (2002) Design of Analog CMOS Integrated Circuits, McGraw Hill.
3. Paul R. Gray, Paul J. Hurst, Stephen H. Lewis and Robert G. Meyer (2001) Analysis and Design of Analog Integrated Circuits, 4th edition, Wiley, John and Sons

b. Recommended Reading

1. Phillip E. Allen and Douglas R. Holberg (2002) CMOS Analog Circuit Design, 2nd edition Oxford University Press
2. R. Jacob Baker (2010) CMOS Circuit Design, Layout, and Simulation, 3rd edition, IEEE Press

c. Website

1. <http://nptel.ac.in/>

10. Course Organization

Course Code	19VLE513A	
Course Title	Analog and Mixed Signal Circuit Design	
Course Leader's Name	As per Timetable	
Course Leader's Contact Details	Phone:	080-49065555
	E-mail:	hod.ec.et@msruas.ac.in
Course Specifications Approval Date	09-July-2019	
Next Course Specifications Review Date	July-2021	

Dean
Faculty of Engineering & Technology
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 058.



Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019

Academic Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 054

Handwritten signature/initials in blue ink.

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

Course Specifications: Programmable Embedded SoCs

Course Title	Programmable Embedded SoCs
Course Code	19VLE514A
Course Type	Professional Core Elective
Department	Electronics and Communication Engineering
Faculty	Engineering and Technology

1. Course Summary

This course deal with the SOC, Embedded IOT design flow and the principle of reconfigurable embedded platforms. In this course students will be taught to develop and program various embedded systems and course using Verilog and system C. Also, here the students will be taught the design and development of IOT architectures on various embedded platform, and various interface protocol required for developing IOT framework and it interface with the cloud.

2. Course Size and Credits:

Number of Credits	04
Credit Structure (Lecture: Tutorial: Practical)	4:0:0
Total Hours of Interaction	60
Number of Weeks in a Semester	15
Department Responsible	Electronics and Communication Engineering
Total Course Marks	100
Pass Criterion	As per the Academic Regulations
Attendance Requirement	As per the Academic Regulations

3. Course Outcomes (COs)

After the successful completion of this course, the student will be able to:

- CO 1. Describe the principles of SOC design flow, reconfigurable computing and reusable cores principles.
- CO 2. Discuss the SOC verification methodologies and the Hardware/ Software co-design methodologies
- CO 3. Discuss the design principles of IOT for Embedded platform
- CO 4. Analyse and develop different layer and communication protocols
- CO 5. Design and prototype the IOT on Embedded platform

4. Course Contents

Unit 1 (Introduction to SoC): SOC Definition, Examples, Platform based SOC design, Architecture of SOC, SOC Design issues, SOC vs. ASIC, ARM architecture.

Unit 2 (SoC Implementation): SOC characteristics, applications, challenges, soft and hard cores, Types of Soc's- EDK, SOC Design flow and Reconfigurable computing: Design flow, codesign flow, Reconfigurable computing, benefits, Reconfigurable design and verification tools, Hardware software Codesign: Design flow, System synthesis, control /data flow models, Levels of abstraction.

Unit 3 (Soc Verification and Testing): Introduction to reuse, General guidelines, Case study, Hardware Software Cosynthesis and Partitioning, Partitioning trend – Approaches, Microblaze,



Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

Picoblaze and Power PC , Xilinx vivado SDK Flow, SOC Verification Methodologies, SOC Testing Techniques.

Unit 4 (Introduction to IoT): IoT-An Architectural Overview– Building an architecture, Main design principles and needed capabilities, An IoT architecture outline, standards considerations. M2M and IoT Technology Fundamentals- Devices and gateways, Local and wide area networking, Data management, Business processes in IoT, Everything as a Service(XaaS), M2M and IoT Analytics, Knowledge Management.

Unit 5 (Programming of IoT Design): IOT Design Architecture, Embedded IOT Protocols, Web of Things and Cloud of Things, Exemplary devices, Raspberry Pi, Raspberry Pi interfaces, Programming Raspberry Pi with Python, Case Study.

5. Course Map (CO-PO-PSO Map)

	Programme Outcomes (POs)												Programme Specific Outcomes (PSOs)		
	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PO-7	PO-8	PO-9	PO-10	PO-11	PO-12	PSO-1	PSO-2	PSO-3
CO-1	3											1	3		1
CO-2	3											1	3		1
CO-3	3											1	3		1
CO-4	3	3	3	1		2	1	2	1			1	3	2	2
CO-5	3	3	3	1		2	1	2	1	3		1	3	2	3

3: Very Strong Contribution, 2: Strong Contribution, 1: Moderate Contribution

6. Course Teaching and Learning Methods

Teaching and Learning Methods	Duration in hours	Total Duration in Hours
Face to Face Lectures		40
Demonstrations		15
1. Demonstration using Videos	15	
2. Demonstration using Physical Models / Systems	00	
3. Demonstration on a Computer	00	
Numeracy		05
1. Solving Numerical Problems	05	
Practical Work		00
1. Course Laboratory	00	
2. Computer Laboratory	00	
3. Engineering Workshop / Course/Workshop / Kitchen	00	
4. Clinical Laboratory	00	
5. Hospital	00	
6. Model Studio	00	
Others		00
1. Case Study Presentation	00	
2. Guest Lecture	00	
3. Industry / Field Visit	00	

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Academic Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 054

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

4. Brain Storming Sessions	00	
5. Group Discussions	00	
6. Discussing Possible Innovations	00	
Term Tests, Laboratory Examination/Written Examination, Presentations		10
Total Duration in Hours		70

7. Course Assessment and Reassessment

The details of the components and subcomponents of course assessment are presented in the Programme Specifications document pertaining to the M.Tech. (VLSI and Nanotechnology) Programme. The procedure to determine the final course marks is also presented in the Programme Specifications document.

The evaluation questions are set to measure the attainment of the COs. In either component (CE or SEE) or subcomponent of CE (SC1, SC2, SC3 or SC4), Cos are assessed as illustrated in the following Table.

Focus of Cos on each Component or Subcomponent of Evaluation					
Subcomponent ▶	Component 1: CE (50% Weightage)				Component 2: SEE (50% Weightage)
	SC1	SC2	SC3	SC4	
Subcomponent Type ▶	Term Test	Assignment	Term Test	Assignment	100 Marks
Maximum Marks ▶	25	25	25	25	
CO-1	X				X
CO-2	X		X		X
CO-3	X	X	X	X	X
CO-4		X	X	X	
CO-5		X		X	

The details of SC1, SC2, SC3 or SC4 are presented in the Programme Specifications Document.

The Course Leader assigned to the course, in consultation with the Head of the Department, shall provide the focus of COs in each component of assessment in the above template at the beginning of the semester.

Course reassessment policies are presented in the Academic Regulations document.

8. Achieving COs

The following skills are directly or indirectly imparted to the students in the following teaching and learning methods:

S. No	Curriculum and Capabilities Skills	How imparted during the course
1.	Knowledge	Classroom Lectures
2.	Understanding	Classroom Lectures, Self-study
3.	Critical Skills	Assignment
4.	Analytical Skills	Assignment
5.	Problem Solving Skills	Assignment and Exam
6.	Practical Skills	Assignment
7.	Group Work	Assignment
8.	Self-Learning	Self-learning
9.	Written Communication Skills	Assignment
10.	Verbal Communication Skills	--

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Academic Registrar
M.S.D. Ramaiah University of Applied Sciences
Bangalore - 560 054

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

11.	Presentation Skills	Assignment
12.	Behavioral Skills	--
13.	Information Management	Assignment
14.	Personal Management	--
15.	Leadership Skills	--

9. Course Resources

a. Essential Reading

1. Course Notes
2. Staustrup and W. Wolf, editors, Hardware/Software Co-Design: Principles and Practice, Kluwer Academic Publishers, 1997
3. Peter Waher, "Learning Internet of Things", PACKT publishing, BIRMINGHAM – MUMBAI

b. Recommended Reading

1. Rochit Rajsuman, System on Chip: Design and Test; Artech House, 2000.
2. Jason Andrews, Co-Verification of Hardware and Software for ARM SoC Design, Elsevier Inc, 2005.

c. Website

1. <http://nptel.ac.in/>

10. Course Organization

Course Code	19VLE514A	
Course Title	Programmable Embedded SoCs	
Course Leader's Name	As per Timetable	
Course Leader's Contact Details	Phone:	080-49065555
	E-mail:	hod.ec.et@msruas.ac.in
Course Specifications Approval Date	09-July-2019	
Next Course Specifications Review Date	July-2021	

Dean
Faculty of Engineering & Technology
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 058.



Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019

Academic Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560058

[Handwritten signature]

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

Course Specifications: MEMS and NEMS

Course Title	MEMS and NEMS
Course Code	19VLE522A
Course Type	Professional Core Elective
Department	Electronics and Communication Engineering
Faculty	Engineering and Technology

1. Course Summary

This course deal with the SOC, Embedded IOT design flow and the principle of reconfigurable embedded platforms. In this course students will be taught to develop and program various embedded systems and course using Verilog and system C. Also, here the students will be taught the design and development of IOT architectures on various embedded platform, and various interface protocol required for developing IOT framework and it interface with the cloud.

2. Course Size and Credits:

Number of Credits	04
Credit Structure (Lecture: Tutorial: Practical)	4:0:0
Total Hours of Interaction	60
Number of Weeks in a Semester	15
Department Responsible	Electronics and Communication Engineering
Total Course Marks	100
Pass Criterion	As per the Academic Regulations
Attendance Requirement	As per the Academic Regulations

3. Course Outcomes (COs)

After the successful completion of this course, the student will be able to:

- CO 1. Gain the physical knowledge underlying the operation principles and design of micro and Nano- systems
- CO 2. Acquire the basics of design and fabrication techniques in MEMS and NEMS
- CO 3. Model and design different types of MEMS and NEMS
- CO 4. Analyze the issues in packaging and choose a suitable packaging technique for various needs
- CO 5. Apply the design and fabrication knowledge for various applications such as Nano machines and robots

4. Course Contents

Unit 1 (Introduction to MEMS and NEMS): Definitions, Taxonomy of Nano-and Microsystems-Synthesis and Design. Classification and considerations, Bio mimetics, Biological analogies, and design-Bio mimetics Fundamentals, Bio mimetics for NEMS and MEMS, Nano-ICs and Nano computer architectures.

Unit 2 (Modelling of MEMS and NEMS): Introduction to modelling, analysis and simulation, basic electro-magnetic with application to MEMS and NEMS, modelling developments of micro-and Nano actuators using electromagnetic-Lumped-parameter mathematical models of MEMS, energy conversion in NEMS and MEMS.

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Academic Registrar
M. S. Ramaiah University of Applied Sciences
Bangalore - 560 054
Page 67 of 94

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

Unit 3 (Fabrication of MEMS): Fabrication processes for silicon -Lithography -Resists and mask formation - Lift-off technique - Etching techniques - Wafer bonding for MEMS - Deposition techniques for thin films in MEMS - Metallization techniques. Thermal oxidation for silicon dioxide - CVD of dielectrics.

Unit 4 (Packaging of MEMS): Role of MEMS packaging, issues -Types of MEMS packaging, packaging techniques -Flip-chip assembly -Ball-grid array -Embedded overlay - Wafer-level packaging and multichip Unit packaging, RF MEMS packaging issues. Reliability and key failure mechanisms -Issues in packaging of microsystems.

Unit 5 (Applications of MEMS and NEMS)

Mechanical MEMS - Thermal MEMS – Magnetic MEMS - RF MEMS - Nano machines and Nano robots.

5. Course Map (CO-PO-PSO Map)

	Programme Outcomes (POs)												Programme Specific Outcomes (PSOs)		
	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PO-7	PO-8	PO-9	PO-10	PO-11	PO-12	PSO-1	PSO-2	PSO-3
CO-1	3											1	3		1
CO-2	3											1	3		1
CO-3	3	3	3	1								1	3		1
CO-4	3	3	3	1		2	1	2	1			1	3	2	2
CO-5	3	3	3	1		2	1	2	1	3		1	3	2	3

3: Very Strong Contribution, 2: Strong Contribution, 1: Moderate Contribution

6. Course Teaching and Learning Methods

Teaching and Learning Methods	Duration in hours	Total Duration in Hours
Face to Face Lectures		40
Demonstrations		05
1. Demonstration using Videos	05	
2. Demonstration using Physical Models / Systems	00	
3. Demonstration on a Computer	00	
Numeracy		15
1. Solving Numerical Problems	15	
Practical Work		00
1. Course Laboratory	00	
2. Computer Laboratory	00	
3. Engineering Workshop / Course/Workshop / Kitchen	00	
4. Clinical Laboratory	00	
5. Hospital	00	
6. Model Studio	00	
Others		00
1. Case Study Presentation	00	
2. Guest Lecture	00	

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Academic Registrar
M.S. Ramaiah University of Applied Sciences
Page 68 of 94
Bangalore - 560 054

Handwritten signature

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

3. Industry / Field Visit	00	
4. Brain Storming Sessions	00	
5. Group Discussions	00	
6. Discussing Possible Innovations	00	
Term Tests, Laboratory Examination/Written Examination, Presentations		10
Total Duration in Hours		70

7. Course Assessment and Reassessment

The details of the components and subcomponents of course assessment are presented in the Programme Specifications document pertaining to the M.Tech. (VLSI and Nanotechnology) Programme. The procedure to determine the final course marks is also presented in the Programme Specifications document.

The evaluation questions are set to measure the attainment of the COs. In either component (CE or SEE) or subcomponent of CE (SC1, SC2, SC3 or SC4), Cos are assessed as illustrated in the following Table.

Focus of Cos on each Component or Subcomponent of Evaluation					
Subcomponent ▶	Component 1: CE (50% Weightage)				Component 2: SEE (50% Weightage)
	SC1	SC2	SC3	SC4	
Subcomponent Type ▶	Term Test	Assignment	Term Test	Assignment	100 Marks
Maximum Marks ▶	25	25	25	25	
CO-1	X				X
CO-2	X		X		X
CO-3	X	X	X	X	X
CO-4		X	X	X	X
CO-5		X		X	X

The details of SC1, SC2, SC3 or SC4 are presented in the Programme Specifications Document.

The Course Leader assigned to the course, in consultation with the Head of the Department, shall provide the focus of COs in each component of assessment in the above template at the beginning of the semester.

Course reassessment policies are presented in the Academic Regulations document.

8. Achieving COs

The following skills are directly or indirectly imparted to the students in the following teaching and learning methods:

S. No	Curriculum and Capabilities Skills	How imparted during the course
1.	Knowledge	Classroom Lectures
2.	Understanding	Classroom Lectures, Self-study
3.	Critical Skills	Assignment
4.	Analytical Skills	Assignment
5.	Problem Solving Skills	Assignment and Exam
6.	Practical Skills	Assignment
7.	Group Work	Assignment
8.	Self-Learning	Self-learning
9.	Written Communication Skills	Assignment



Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

10.	Verbal Communication Skills	--
11.	Presentation Skills	Assignment
12.	Behavioral Skills	--
13.	Information Management	Assignment
14.	Personal Management	--
15.	Leadership Skills	--

9. Course Resources

a. Essential Reading

1. Course Notes
2. S. Gopala Krishnan, Vijay.K, K.J.Vinoy (2015), Smart Material Systems and MEMS: Design and Development methodologies, Wiley Publisher.
3. Chang Liu (2011), Foundations of MEMS, Pearson Education, 2nd edition

b. Recommended Reading

1. Korvink J.G, Oliver Paul (2006), MEMS Practical guide to design, analysis and Applications, Springer
2. Pelesko J.A and D. H. Bernstein (2002), Modelling MEMS and NEMS. Chapman & Hall/ CRC.

c. Website

1. <http://nptel.ac.in/>

10. Course Organization

Course Code	19VLE522A	
Course Title	MEMS and NEMS	
Course Leader's Name	As per Timetable	
Course Leader's Contact Details	Phone:	080-49065555
	E-mail:	hod.ec.et@msruas.ac.in
Course Specifications Approval Date	09-July-2019	
Next Course Specifications Review Date	July-2021	

Dean
 Faculty of Engineering & Technology
 M.S. Ramaiah University of Applied Sciences
 Bangalore - 560 058.

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019




 Academic Registrar
 M.S. Ramaiah University of Applied Sciences
 Bangalore - 560 054

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

Course Specifications: Advanced Nano Materials and Applications

Course Title	Advanced Nano Materials and Applications
Course Code	19VLE523A
Course Type	Professional Core Elective
Department	Electronics and Communication Engineering
Faculty	Engineering and Technology

1. Course Summary

The purpose of this course is to provide knowledge on Nanomaterials used Energy Devices, Electrical and Electronics Industry, Biological Applications, Textiles and Defence.

2. Course Size and Credits:

Number of Credits	04
Credit Structure (Lecture: Tutorial: Practical)	4:0:0
Total Hours of Interaction	60
Number of Weeks in a Semester	15
Department Responsible	Electronics and Communication Engineering
Total Course Marks	100
Pass Criterion	As per the Academic Regulations
Attendance Requirement	As per the Academic Regulations

3. Course Outcomes (COs)

After the successful completion of this course, the student will be able to:

- CO 1. Elucidate on advantages of nanotechnology-based applications in each industry
- CO 2. Provide instances of contemporary industrial applications of nanotechnology
- CO 3. Provide an overview of future technological advancements and increasing role of nanotechnology in textile industry
- CO 4. Provide an overview of future technological advancements and increasing role of nanotechnology in defence industry
- CO 5. Provide an overview of future technological advancements and increasing role of nanotechnology in electrical and electronics industry

4. Course Contents

Unit 1 (Nano materials for Fuel Cell Applications): Electronic and electrochemical energy devices Conversion Systems, Energy Storage Systems, Primary and Secondary Batteries (Lithium ion Batteries), Cathode and anode materials, Nanostructured Carbon based materials, Nano-Oxides, Chalcogenides, Novel hybrid electrode materials, Nanomaterials for capacitors: Electrochemical supercapacitors, Nanostructured carbon based materials, Conducting polymers and their applications in corrosion protection, Future trends, Principles of fuel cells, Nanomaterials design for Proton exchange membrane fuel cells (PEMFC); Direct methanol fuel cells (DMFC); Solid-oxide fuel cells (SOFC), Future trends.

Unit 2 (Nano materials for Nanosensor Applications): Advantages of nano electrical and electronic devices, Electronic circuit chips, Nanosensors and actuators, Optical switches: Diodes and Nano-wire

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019

M.S. Ramalah University of Applied Sciences
Bangalore - 560 054

Academic Registrar
M.S. Ramalah University of Applied Sciences
Bangalore - 560 054

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

transistors, Memory storage, Lighting and displays, Filters (IR blocking), Quantum computers, Energy devices, Medical diagnosis, Conductive additives, Lead-free solder, Nanocoatings: EMI shielding, Magnetic Applications, Photonic Applications

Unit 3 (Nano material for Medical Applications): Interaction of light with tissues: Nature of Optical interactions, The interface of bioscience, nanotechnology and photonics: Semiconductor quantum dots for bioimaging, Metallic nanoparticles and nanorods for Biosensing, Bioinspired materials, Tissue Engineering application, Fundamentals of Drug Nanoparticles: Production, Size, Surface area, Suspension and Settling, Delivery of Nanoparticles: Brain Delivery, Ocular Drug Delivery, Gene Delivery Systems, Carriers in Cancer Therapy, Cardiovascular System, Vascular Delivery to the Lungs, Targeting Lymphatics.

Unit 4 (Nano materials for Textile Applications): Nanofibre production: Electrospinning, Nano-fillers embedded polypropylene fibers, Bionics – Swim-suits with shark-skin effect, Soil repellence, Nano finishing in textiles: UV resistant, anti-bacterial, hydrophilic, self-cleaning, flame retardant finish, Modern textiles: Lightweight bulletproof vests and shirts, Colour changing property, Waterproof and Germ proof clothes, Nanopolymers in medical textiles.

Unit 5 (Nano material for Military Applications): Artificial intelligence materials, Smart materials usage in structures, health monitoring of defense systems, nanomaterials for propulsion systems, Camouflage distributed sensors, Soldier systems - Implanted systems, Body manipulation.

5. Course Map (CO-PO-PSO Map)

	Programme Outcomes (POs)												Programme Specific Outcomes (PSOs)		
	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PO-7	PO-8	PO-9	PO-10	PO-11	PO-12	PSO-1	PSO-2	PSO-3
CO-1	3											1	3		1
CO-2	3											1	3		1
CO-3	3											1	3		1
CO-4	3	3	3	1		2	1	2	1			1	3	2	2
CO-5	3	3	3	1		2	1	2	1	3		1	3	2	3

3: Very Strong Contribution, 2: Strong Contribution, 1: Moderate Contribution

6. Course Teaching and Learning Methods

Teaching and Learning Methods	Duration in hours	Total Duration in Hours
Face to Face Lectures		45
Demonstrations		15
1. Demonstration using Videos	15	
2. Demonstration using Physical Models / Systems	00	
3. Demonstration on a Computer	00	
Numeracy		00
1. Solving Numerical Problems	00	
Practical Work		00
1. Course Laboratory	00	
2. Computer Laboratory	00	
3. Engineering Workshop / Course/Workshop /	00	

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Academic Registrar
M.S.R. Ramiah University of Applied Sciences
Bangalore - 560 054
Page 72 of 94

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

Kitchen		
4. Clinical Laboratory	00	
5. Hospital	00	
6. Model Studio	00	
Others		00
1. Case Study Presentation	00	
2. Guest Lecture	00	
3. Industry / Field Visit	00	
4. Brain Storming Sessions	00	
5. Group Discussions	00	
6. Discussing Possible Innovations	00	
Term Tests, Laboratory Examination/Written Examination, Presentations		10
Total Duration in Hours		70

7. Course Assessment and Reassessment

The details of the components and subcomponents of course assessment are presented in the Programme Specifications document pertaining to the M.Tech. (VLSI and Nanotechnology) Programme. The procedure to determine the final course marks is also presented in the Programme Specifications document.

The evaluation questions are set to measure the attainment of the COs. In either component (CE or SEE) or subcomponent of CE (SC1, SC2, SC3 or SC4), Cos are assessed as illustrated in the following Table.

Focus of Cos on each Component or Subcomponent of Evaluation					
Subcomponent ▶	Component 1: CE (50% Weightage)				Component 2: SEE (50% Weightage)
	SC1	SC2	SC3	SC4	
Subcomponent Type ▶	Term Test	Assignment	Term Test	Assignment	100 Marks
Maximum Marks ▶	25	25	25	25	
CO-1	X				X
CO-2	X	X	X		X
CO-3	X	X	X	X	X
CO-4		X	X	X	X
CO-5		X	X	X	X

The details of SC1, SC2, SC3 or SC4 are presented in the Programme Specifications Document.

The Course Leader assigned to the course, in consultation with the Head of the Department, shall provide the focus of COs in each component of assessment in the above template at the beginning of the semester.

Course reassessment policies are presented in the Academic Regulations document.

8. Achieving COs

The following skills are directly or indirectly imparted to the students in the following teaching and learning methods:

S. No	Curriculum and Capabilities Skills	How imparted during the course
1.	Knowledge	Classroom Lectures



Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

2.	Understanding	Classroom Lectures, Self-study
3.	Critical Skills	Assignment
4.	Analytical Skills	Assignment
5.	Problem Solving Skills	Assignment and Exam
6.	Practical Skills	Assignment
7.	Group Work	Assignment
8.	Self-Learning	Self-learning
9.	Written Communication Skills	Assignment
10.	Verbal Communication Skills	--
11.	Presentation Skills	Assignment
12.	Behavioral Skills	--
13.	Information Management	Assignment
14.	Personal Management	--
15.	Leadership Skills	--

9. Course Resources

a. Essential Reading

1. Course Notes
2. Bharat Bhushan, "Handbook of Nanotechnology", Springer, 2010.
3. Jennifer Kuzma and Peter VerHage, "Nanotechnology in agriculture and food production", Woodrow Wilson International Center, 2006.

b. Recommended Reading

1. Neelina H. Malsch (Ed.), "Biomedical Nanotechnology", CRC Press, 2005.
2. Maqhong fan, C.P. Huang, Alan E. Bland "Environanotechnology", Elsevier, 2010

c. Website

1. <http://nptel.ac.in/>

10. Course Organization

Course Code	19VLE523A	
Course Title	Advanced Nano Materials and Applications	
Course Leader's Name	As per Timetable	
Course Leader's Contact Details	Phone:	080-49065555
	E-mail:	hod.ec.et@msruas.ac.in
Course Specifications Approval Date	09-July-2019	
Next Course Specifications Review Date	July-2021	

Dean
Faculty of Engineering & Technology
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 058.



Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

Course Specifications: Quantum Computing and Communication

Course Title	Quantum Computing and Communication
Course Code	19VLE524A
Course Type	Professional Core Elective
Department	Electronics and Communication Engineering
Faculty	Engineering and Technology

1. Course Summary

The main aim of this course is to develop amongst students an understanding of the key concepts and principles that underpin the emerging world of quantum communications and computing. The students are introduced with the concepts and basic mathematics behind quantum computers. The course also focuses on quantum communication, an essential component of future quantum information processing, and quantum cryptography, widely expected to be the first practical application for quantum information technology.

2. Course Size and Credits:

Number of Credits	04
Credit Structure (Lecture: Tutorial: Practical)	4:0:0
Total Hours of Interaction	60
Number of Weeks in a Semester	15
Department Responsible	Electronics and Communication Engineering
Total Course Marks	100
Pass Criterion	As per the Academic Regulations
Attendance Requirement	As per the Academic Regulations

3. Course Outcomes (COs)

After the successful completion of this course, the student will be able to:

- CO 1. Discuss the theory, concepts and challenges of quantum mechanics as applied to computing and communications.
- CO 2. Design and simulate the quantum circuits and algorithms
- CO 3. Discuss the fundamentals of quantum computation identify the requirements for physical systems to be used as quantum computers;
- CO 4. Design and simulate the behavior of quantum communication networks
- CO 5. Analyze and determine the performance of a quantum network through specific performance metrics

4. Course Contents

Unit 1 (Introduction to Quantum Computing): Quantitative measure of information –Shannon's coding theorem- information management technology, Qubits -History of quantum computing and communication. Classical and quantum computational models. Algorithm complexity –Turing machine. Deterministic and probabilistic Turing machine- Circuit model for computation and computational complexity and related issues. Quantum mechanics and algebra for quantum computing.



Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

Unit 2 (Quantum Circuits): Single, two and three Qubit gates- Quantum circuits –Measures of quality of circuit and optimization rules. Quantum algorithms –Deutsch Jozsa, Grover's and Simon's algorithm –Shor's algorithm.

Unit 3 (Quantum Error Models): Error model- Classical and quantum error- correction of quantum error- phase flip error- Shor code. Fault tolerant quantum computation, Threshold theorem for quantum computation.

Unit 4 (Teleportation): Teleportation types –schemes for perfect teleportation, Probabilistic teleportation –controlled teleportation, modified teleportation schemes –super dense coding.

Unit 5 (Quantum Cryptography): Different aspects of quantum cryptography-Quantum key distribution (QKD). Different protocols -1, 4, 5. GV protocol-ping pong protocol and modified ping pong protocol. Data link layer (DLL) and modified DLL protocols. DSQC and DSDC protocol. Quantum dialogue and quantum secret sharing.

5. Course Map (CO-PO-PSO Map)

	Programme Outcomes (POs)												Programme Specific Outcomes (PSOs)		
	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PO-7	PO-8	PO-9	PO-10	PO-11	PO-12	PSO-1	PSO-2	PSO-3
CO-1	3											1	3		1
CO-2	3											1	3		1
CO-3	3											1	3		1
CO-4	3	3	3	1		2	1	2	1			1	3	2	2
CO-5	3	3	3	1		2	1	2	1	3		1	3	2	3

3: Very Strong Contribution, 2: Strong Contribution, 1: Moderate Contribution

6. Course Teaching and Learning Methods

Teaching and Learning Methods	Duration in hours	Total Duration in Hours
Face to Face Lectures		40
Demonstrations		15
1. Demonstration using Videos	15	
2. Demonstration using Physical Models / Systems	00	
3. Demonstration on a Computer	00	
Numeracy		05
1. Solving Numerical Problems	05	
Practical Work		00
1. Course Laboratory	00	
2. Computer Laboratory	00	
3. Engineering Workshop / Course/Workshop / Kitchen	00	
4. Clinical Laboratory	00	
5. Hospital	00	
6. Model Studio	00	
Others		00



Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

1. Case Study Presentation	00	
2. Guest Lecture	00	
3. Industry / Field Visit	00	
4. Brain Storming Sessions	00	
5. Group Discussions	00	
6. Discussing Possible Innovations	00	
Term Tests, Laboratory Examination/Written Examination, Presentations	10	
Total Duration in Hours	70	

7. Course Assessment and Reassessment

The details of the components and subcomponents of course assessment are presented in the Programme Specifications document pertaining to the M.Tech. (VLSI and Nanotechnology) Programme. The procedure to determine the final course marks is also presented in the Programme Specifications document.

The evaluation questions are set to measure the attainment of the COs. In either component (CE or SEE) or subcomponent of CE (SC1, SC2, SC3 or SC4), Cos are assessed as illustrated in the following Table.

Focus of Cos on each Component or Subcomponent of Evaluation					
Subcomponent ▶	Component 1: CE (50% Weightage)				Component 2: SEE (50% Weightage)
	SC1	SC2	SC3	SC4	
Subcomponent Type ▶	Term Test	Assignment	Term Test	Assignment	100 Marks
Maximum Marks ▶	25	25	25	25	
CO-1	X				X
CO-2	X	X		X	X
CO-3			X		X
CO-4		X	X	X	X
CO-5		X	X	X	X

The details of SC1, SC2, SC3 or SC4 are presented in the Programme Specifications Document.

The Course Leader assigned to the course, in consultation with the Head of the Department, shall provide the focus of COs in each component of assessment in the above template at the beginning of the semester.

Course reassessment policies are presented in the Academic Regulations document.

8. Achieving COs

The following skills are directly or indirectly imparted to the students in the following teaching and learning methods:

S. No	Curriculum and Capabilities Skills	How imparted during the course
1.	Knowledge	Classroom Lectures
2.	Understanding	Classroom Lectures, Self-study
3.	Critical Skills	Assignment
4.	Analytical Skills	Assignment
5.	Problem Solving Skills	Assignment and Exam
6.	Practical Skills	Assignment
7.	Group Work	Assignment

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Academic Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 084
Page 77 of 94

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

8.	Self-Learning	Self-learning
9.	Written Communication Skills	Assignment
10.	Verbal Communication Skills	--
11.	Presentation Skills	Assignment
12.	Behavioral Skills	--
13.	Information Management	Assignment
14.	Personal Management	--
15.	Leadership Skills	--

9. Course Resources

a. Essential Reading

1. Course Notes
2. Anirban Pathakels (2013), Elements of Quantum Computation and Quantum Communication, CRC Press; 1 edition
3. Quantum Computation and Quantum Information, 2010, Michael A. Nielsen, Isaac L. Chuang, Cambridge University Press; Anniversary edition

b. Recommended Reading

1. Pavicic Mladen (2007), Quantum Computation and Quantum Communication Theory and Experiments ,new age publishers

c. Website

1. <http://nptel.ac.in/>

10. Course Organization

Course Code	19VLE524A	
Course Title	Quantum Computing and Communication	
Course Leader's Name	As per Timetable	
Course Leader's Contact Details	Phone:	080-49065555
	E-mail:	hod.ec.et@msruas.ac.in
Course Specifications Approval Date	09-July-2019	
Next Course Specifications Review Date	July-2021	

Dean
 Faculty of Engineering & Technology
 M.S. Ramaiah University of Applied Sciences
 Bangalore - 560 058.

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Academic Registrar
 M.S. Ramaiah University of Applied Sciences
 Bangalore - 560 054
 Page 78 of 94

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

Course Specifications: Value Education

Course Title	Value Education
Course Code	19FETS10A
Course Type	Ability Enhanced Compulsory
Department	Electronics and Communication Engineering
Faculty	Engineering and Technology

1. Course Summary

This course aims at sensitizing students to learn the importance of value education. It gives an insight about the Universal Brotherhood.

2. Course Size and Credits:

Number of Credits	00
Credit Structure (Lecture: Tutorial: Practical)	0:0:0
Total Hours of Interaction	15
Number of Weeks in a Semester	15
Department Responsible	Directorate of Transferable Skills and Leadership Development
Total Course Marks	25
Pass Criterion	As per the Academic Regulations
Attendance Requirement	As per the Academic Regulations

3. Course Outcomes (COs)

After the successful completion of this course, the student will be able to:

CO-1. Discuss the role of Values and Ethics in Self-Development

CO-2. Appreciate the importance of Universal Brotherhood

4. Course Contents

Unit 1 (Communication – Values, Ethics and Judgements): Values, Ethics and Self-Development; Awareness of self-destructive habits, Power of faith, Positive Thinking Value judgements – Stereotypes, prejudices and biases

Unit 2 (Communication – Sense of Duty): Sense of duty, Self-reliance, Confidence, Concentration, Discipline, Honesty, Truthfulness. National Unity, Patriotism, Love for nature

Unit 3 (Communication – Character Development): Universal brotherhood and religious tolerance. Character and Competence –Rational Thinking vs Blind faith



Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

5. Course Map (CO-PO-PSO Map)

	Programme Outcomes (POs)												Programme Specific Outcomes (PSOs)		
	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PO-7	PO-8	PO-9	PO-10	PO-11	PO-12	PSO-1	PSO-2	PSO-3
CO-1							2	3				2		2	3
CO-2	2								2			3	2		3
3: Very Strong Contribution, 2: Strong Contribution, 1: Moderate Contribution															

6. Course Teaching and Learning Methods

Teaching and Learning Methods	Duration in hours	Total Duration in Hours
Face to Face Lectures		09
Demonstrations		00
1. Demonstration using Videos	00	
2. Demonstration using Physical Models / Systems	00	
3. Demonstration on a Computer	00	
Numeracy		00
1. Solving Numerical Problems	00	
Practical Work		
1. Course Laboratory	00	
2. Computer Laboratory	00	
3. Engineering Workshop / Course/Workshop / Kitchen	00	
4. Clinical Laboratory	00	
5. Hospital	00	
6. Model Studio	00	
Others		06
1. Case Study Presentation	02	
2. Guest Lecture	00	
3. Industry / Field Visit	00	
4. Brain Storming Sessions	00	
5. Group Discussions	04	
6. Discussing Possible Innovations	00	
In-class assessments, Term Tests, Laboratory Examination/Written Examination, Presentations		03
Total Duration in Hours		18

7. Course Assessment and Reassessment

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



M.S.R.
Academic Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 054

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

The details of the components and subcomponents of course assessment are presented in the Programme Specifications document pertaining to the M.Tech. Programme. The procedure to determine the final course marks is also presented in the Programme Specifications document. The evaluation questions are set to measure the attainment of the COs. In either component (CE or SEE) or subcomponent of CE (SC1, SC2, SC3 or SC4), COs are assessed as illustrated in the following Table.

Focus of CO's on each Component or Subcomponent of Evaluation:		
	Component 1: CE (100% Weightage)	Component 2: SEE (0% Weightage)
Subcomponent▶	SC1	0 Marks
Subcomponent Type ▶	In-Class Assessment	
Maximum Marks▶	25	
CO-1	X	
CO-2	X	

The Course Leader assigned to the course, in consultation with the Head of the Department, shall provide the focus of COs in each component of assessment in the above template at the beginning of the semester.

Course reassessment policies are presented in the Academic Regulations document.

8. Achieving COs

The following skills are directly or indirectly imparted to the students in the following teaching and learning methods:

S. No	Curriculum and Capabilities Skills	How imparted during the course
1.	Knowledge	Face to face lectures
2.	Understanding	Face to face lectures, group discussions
3.	Critical Skills	--
4.	Analytical Skills	Face to face lectures, activities, , group discussions, assignment
5.	Problem Solving Skills	--
6.	Practical Skills	Face to face lectures, activities, , group discussions, course work
7.	Group Work	Course work, practice, assignment, group discussion
8.	Self-Learning	Course work, practice, assignment, group discussion
9.	Written Communication Skills	Face to face lectures, Course work, practice, assignment, group discussion
10.	Verbal Communication Skills	Face to face lectures, Course work, practice, assignment, group discussion
11.	Presentation Skills	--
12.	Behavioral Skills	Course work, practice, assignment, group discussion, presentation practice, role plays
13.	Information Management	Assignment

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Handwritten signature

Academic Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 054

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

14.	Personal Management	--
15.	Leadership Skills	--

9. Course Resources

- a. Essential Reading
 - 1. Class Notes
- b. Recommended Reading
- c. Magazines and Journals
- d. Websites
- e. Other Electronic Resources
 - 1. Electronic resources on the course area are available on RUAS library

10. Course Organization

Course Code	19FET510A	
Course Title	Value Education	
Course Leader's Name	As per Timetable	
Course Leader's Contact Details	Phone:	+91-80-453666666
	E-mail:	director.tsld@msruas.ac.in
Course Specifications Approval Date	24-JULY-2019	
Next Course Specifications Review Date	July-2021	

???

Dean
 Faculty of Engineering & Technology
 M.S. Ramaiah University of Applied Sciences
 Bangalore - 560 058.

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



Hlo

Academic Registrar
 M.S. Ramaiah University of Applied Sciences
 Bangalore - 560 058

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

Course Specifications: Group Project

Course Title	Group Project
Course Code	19VLP522A
Course Type	Project
Department	Electronics and Communication Engineering
Faculty	Engineering and Technology

1. Course Summary

This course is intended to apply and synergize the learning outcomes of M.Tech. in VLSI and Nanotechnology programme through a group project. The group project will focus on application of VLSI and FPGA tool to build a prototype of a chosen project idea. This course will enable the students to gain practical experience of working in a project mode, requiring interactions with the domain specialist for the project undertaken. The significant feature of the project will be the demonstration of its applicability and usefulness to the society.

2. Course Size and Credits:

Number of Credits	08
Credit Structure (Lecture: Tutorial: Practical)	0:0:8
Total Hours of Interaction	25
Number of Weeks in a Semester	15
Department Responsible	Electronics and Communication Engineering
Total Course Marks	200
Pass Criterion	As per the Academic Regulations
Attendance Requirement	As per the Academic Regulations

3. Course Outcomes (COs)

After the successful completion of this course, the student will be able to:

- CO 1. Define aim and objectives of the chosen project idea and explain its applications
- CO 2. Arrive at various technical specifications to be targeted while executing the project
- CO 3. Specify the methodologies/procedure/methods for the design and implementation of the project
- CO 4. Demonstrate /present a prototype of the implemented project
- CO 5. Work as team, develop leadership and project management skills

4. Course Contents

Team building, Team work and Leadership skills, Preparing design specifications, design, analysis and synthesis, design evaluation, Costing, Finance Management, Project management, Procurement, prototype building and related manufacturing methods, Preparing and presenting audio-visual and verbal presentations and preparing written documents.

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



[Handwritten Signature]
Academic Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 054

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

5. Course Map (CO-PO-PSO Map)

	Programme Outcomes (POs)												Programme Educational Outcomes (PEOs)		
	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PO-7	PO-8	PO-9	PO-10	PO-11	PO-12	PEO-1	PEO-2	PEO-3
CO-1	3	3	3	3	3	2	1	2	1		2	1	3	3	2
CO-2	3	3	3	3	3	2	1	2	1	3	2	1	3	3	3
CO-3	3	3	3	3	3	2	1	2	1		2	1	3	3	2
CO-4	3	3	3	3	3	2	1	2	1		2	1	3	3	2
CO-5	3	3	3	3	3	2	1	2	1	3	2	1	3	3	3

3: Very Strong Contribution, 2: Strong Contribution, 1: Moderate Contribution

6. Course Teaching and Learning Methods

Teaching and Learning Methods	Duration in hours	Total Duration in Hours
Face to Face Lectures		0
Demonstrations		0
1. Demonstration using Videos	00	
2. Demonstration using Physical Models / Systems	00	
3. Demonstration on a Computer	00	
Numeracy		0
1. Solving Numerical Problems	00	
Practical Work		200
1. Course Laboratory	150	
2. Computer Laboratory	50	
3. Engineering Workshop / Course/Workshop / Kitchen	00	
4. Clinical Laboratory	00	
5. Hospital	00	
6. Model Studio	00	
Others		25
1. Case Study Presentation	00	
2. Guest Lecture	00	
3. Industry / Field Visit	10	
4. Brain Storming Sessions	10	
5. Group Discussions	00	
6. Discussing Possible Innovations	5	
Term Tests, Laboratory Examination/Written Examination, Presentations		10
Total Duration in Hours		235

7. Course Assessment and Reassessment

The details of the components and subcomponents of course assessment are presented in the Programme Specifications document pertaining to the M.Tech. Programme. The procedure to determine the final course marks is also presented in the Programme Specifications document.

The evaluation questions are set to measure the attainment of the COs. In either component (CE or SEE) or subcomponent of CE (SC1, SC2, SC3 or SC4), COs are assessed as illustrated in the following Table.

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



M.S. Ramiah
Academic Registrar
M.S. Ramiah University of Applied Sciences
Bangalore
Page 88 of 94
054

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

Focus of CO's on each Component or Subcomponent of Evaluation:

Focus of COs on each Component or Subcomponent of Evaluation		
	Component 1: (50% Weightage)	Component 2: (50% Weightage)
Component Type ▶	Presentation	Report
Maximum Marks ▶	50	50 Marks
CO-1	☐	☐
CO-2	☐	☐
CO-3	☐	☐
CO-4	☐	☐
CO-5	☐	☐
The details of SC1, SC2, SC3 or SC4 are presented in the Programme Specifications Document.		

The Course Leader / Mentor / Guide /

igned to the course, in consultation with the Head of the Department, shall provide the focus of COs in each component of assessment in the above template at the beginning of the semester. Course reassessment policies are presented in the Academic Regulations document.

8. Achieving COs

The following skills are directly or indirectly imparted to the students in the following teaching and learning methods:

S. No	Curriculum and Capabilities Skills	How imparted during the course
1.	Knowledge	Self-study
2.	Understanding	Self-study
3.	Critical Skills	Report
4.	Analytical Skills	Report
5.	Problem Solving Skills	Modelling and Simulation
6.	Practical Skills	Modelling and Simulation
7.	Group Work	--
8.	Self-Learning	Self-study
9.	Written Communication Skills	Report
10.	Verbal Communication Skills	Presentation
11.	Presentation Skills	Presentation
12.	Behavioral Skills	Meetings with Mentor, Presentation
13.	Information Management	Report
14.	Personal Management	--
15.	Leadership Skills	--

9. Course Resources

a. Essential Reading

Assigned reading relevant to the group project

b. Magazines and Journals

Will be suitably advised based on chosen topic

c. Websites

Will be suitably advised based on chosen topic

d. Other Electronic Resources

Will be suitably advised based on chosen topic

10. Course Organization

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



H.O.
Academic Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 054

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

Course Code	19VLP522A	
Course Title	Group Project	
Course Leader's Name	As per Timetable	
Course Leader's Contact Details	Phone:	+91-80-453666666
	E-mail:	director.tsld@msruas.ac.in
Course Specifications Approval Date	09-July-2019	
Next Course Specifications Review Date	July-2021	

Dean
Faculty of Engineering & Technology
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 058.

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



[Signature]
Academic Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 054

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

Course Specifications: Dissertation and Publication

Course Title	Dissertation and Publication
Course Code	19VLP523A
Course Type	Project
Department	Electronics and Communication Engineering
Faculty	Engineering and Technology

1. Course Summary

This course is intended to give an insight to the students on application of principles of research methodology, preparation of research project proposal, research project management, execution of research project and effective technical communication and presentation. It also emphasizes the need and the relevance of a structured approach to identify a research topic and undertake research. This course provides an opportunity for students to apply theories and techniques learnt during programme work. It involves in-depth work in the chosen area of study. The student is required to carry out original research, author a journal paper for publication. The student is also required to submit the research paper to a journal approved by the department and make a presentation to the examiners in the faculty.

2. Course Size and Credits:

Number of Credits	24
Credit Structure (Lecture: Tutorial: Practical)	0:0:24
Total Hours of Interaction	60
Number of Weeks in a Semester	15
Department Responsible	Electronics and Communication Engineering
Total Course Marks	400
Pass Criterion	As per the Academic Regulations
Attendance Requirement	As per the Academic Regulations

3. Course Outcomes (COs)

After the successful completion of this course, the student will be able to:

- CO 1. Critically review scholarly literature collected from various sources for the project purpose and formulate a research problem
- CO 2. Prepare and present a research proposal
- CO 3. Conduct research to achieve research objectives
- CO 4. Propose new ideas/methodologies or procedures for further improvement of the research undertaken
- CO 5. Create research document and write research papers for publications
- CO 6. Defend the research findings in front of scholarly audiences

4. Course Contents

Research Methodology, Information search, retrieval and review, Project definition and project planning, Use of conceptual models and frameworks Problem solving and Evaluation Interpretations and drawing, conclusions Proposing ideas or methods for further work Thesis writing, Oral presentation, Authoring Research paper.



Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

5. Course Map (CO-PO-PSO Map)

	Programme Outcomes (POs)												Programme Educational Outcomes (PEOs)		
	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PO-7	PO-8	PO-9	PO-10	PO-11	PO-12	PEO-1	PEO-2	PEO-3
CO-1	3	3	3	3	3	2	1	2	1		2	1	3	3	2
CO-2	3	3	3	3	3	2	1	2	1	3	2	1	3	3	3
CO-3	3	3	3	3	3	2	1	2	1		2	1	3	3	2
CO-4	3	3	3	3	3	2	1	2	1		2	1	3	3	2
CO-5	3	3	3	3	3	2	1	2	1	3	2	1	3	3	3
CO-6	3	3	3	3	3	2	1	2	1	3	2	1	3	3	3

3: Very Strong Contribution, 2: Strong Contribution, 1: Moderate Contribution

6. Course Teaching and Learning Methods

Teaching and Learning Methods	Duration in hours	Total Duration in Hours
Face to Face Lectures		0
Demonstrations		0
1. Demonstration using Videos	00	
2. Demonstration using Physical Models / Systems	00	
3. Demonstration on a Computer	00	
Numeracy		0
1. Solving Numerical Problems	00	
Practical Work		300
1. Course Laboratory	200	
2. Computer Laboratory	100	
3. Engineering Workshop / Course/Workshop / Kitchen	00	
4. Clinical Laboratory	00	
5. Hospital	00	
6. Model Studio	00	
Others		60
1. Case Study Presentation	00	
2. Guest Lecture	00	
3. Industry / Field Visit	10	
4. Brain Storming Sessions	20	
5. Group Discussions	00	
6. Discussing Possible Innovations	30	
Term Tests, Laboratory Examination/Written Examination, Presentations		10
Total Duration in Hours		370

7. Course Assessment and Reassessment

The details of the components and subcomponents of course assessment are presented in the Programme Specifications document pertaining to the M.Tech. Programme. The procedure to determine the final course marks is also presented in the Programme Specifications document.



Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

The evaluation questions are set to measure the attainment of the COs. In either component (CE or SEE) or subcomponent of CE (SC1, SC2, SC3 or SC4), COs are assessed as illustrated in the following Table.

Focus of CO's on each Component or Subcomponent of Evaluation:

Focus of COs on each Component or Subcomponent of Evaluation		
	Component 1: (50% Weightage)	Component 2: (50% Weightage)
Component Type ▶	Presentation	Dissertation + Publication
Maximum Marks ▶	200 Marks	200 Marks
CO-1	<input type="checkbox"/>	<input type="checkbox"/>
CO-2	<input type="checkbox"/>	<input type="checkbox"/>
CO-3	<input type="checkbox"/>	<input type="checkbox"/>
CO-4	<input type="checkbox"/>	<input type="checkbox"/>
CO-5	<input type="checkbox"/>	<input type="checkbox"/>
CO-6	<input type="checkbox"/>	<input type="checkbox"/>
The details of SC1, SC2, SC3 or SC4 are presented in the Programme Specifications Document.		

The Course Leader / Mentor / Guide / assigned to the course, in consultation with the Head of the Department, shall provide the focus of COs in each component of assessment in the above template at the beginning of the semester.

Course reassessment policies are presented in the Academic Regulations document.

8. Achieving COs

The following skills are directly or indirectly imparted to the students in the following teaching and learning methods:

S. No	Curriculum and Capabilities Skills	How imparted during the course
1.	Knowledge	Self-study
2.	Understanding	Self-study
3.	Critical Skills	Report
4.	Analytical Skills	Report
5.	Problem Solving Skills	Modelling and Simulation
6.	Practical Skills	Modelling and Simulation
7.	Group Work	--
8.	Self-Learning	Self-study
9.	Written Communication Skills	Report
10.	Verbal Communication Skills	Presentation
11.	Presentation Skills	Presentation
12.	Behavioral Skills	Meetings with Mentor, Presentation
13.	Information Management	Report
14.	Personal Management	--
15.	Leadership Skills	--

9. Course Resources

a. Essential Reading

Assigned reading relevant to the group project

b. Magazines and Journals

Will be suitably advised based on chosen topic

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019



HLO
Academic Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 054

Programme Structure and Course Details of M.Tech in VLSI and Nanotechnology 2019 onwards

c. Websites

Will be suitably advised based on chosen topic

d. Other Electronic Resources

Will be suitably advised based on chosen topic

10. Course Organization

Course Code	19VLP523A	
Course Title	Dissertation and Publication	
Course Leader's Name	As per Timetable	
Course Leader's Contact Details	Phone:	+91-80-45366666
	E-mail:	director.tsld@msruas.ac.in
Course Specifications Approval Date	09-July-2019	
Next Course Specifications Review Date	July-2021	

Dean
Faculty of Engineering & Technology
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 058.


Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 054


Academic Registrar
M.S. Ramaiah University of Applied Sciences
Bangalore - 560 054

Approval: Agenda No. 1, Academic Council Meeting on 12-September-2019